NXM5005

VCM Driver without Hall sensor

General Description

The NXM5005 is a one chip hall sensor driver.
It includes ADC, controller and actuator.
The NXM5005 has rotational movement detector in magnetic embedded system.
Because of that, It can operate with very high accuracy.
The Rotation movement detection method is a distinctive algorithm of NEXTLab.

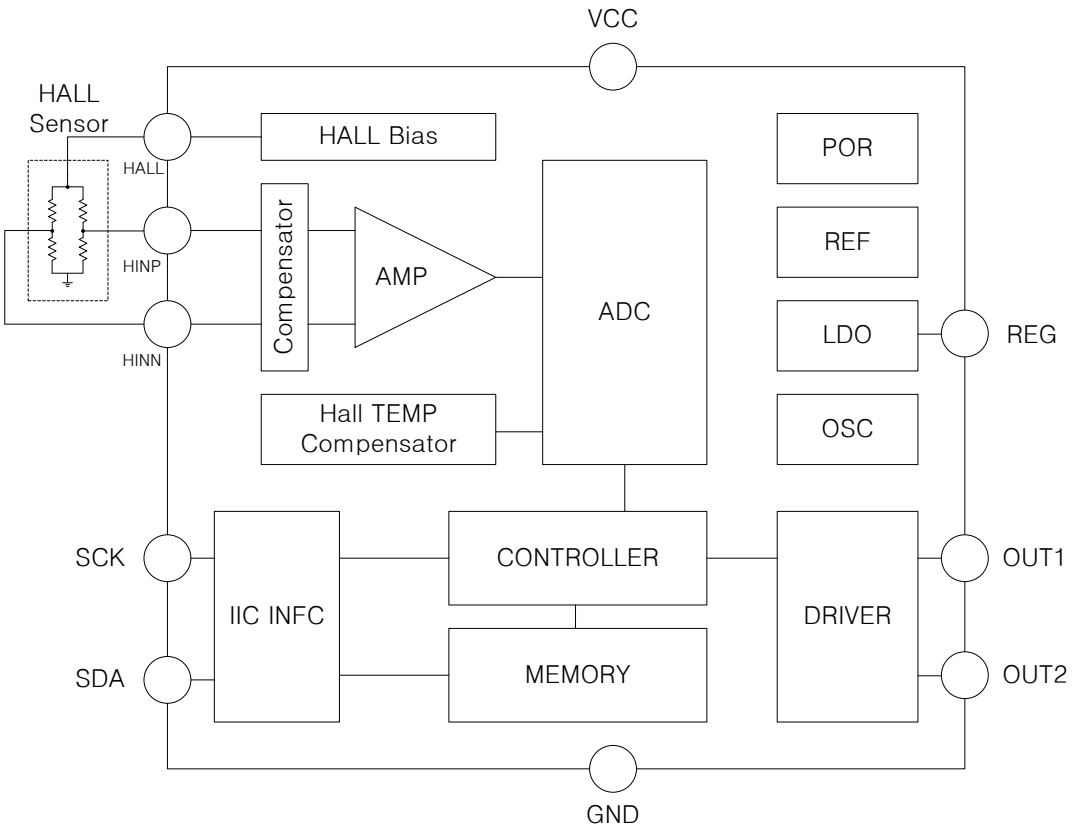
Feature

- Supply voltage : 1.8V ~ 3.6V
- IIC Interface : standard/fast mode
  Default Slave address E0/E1 (W/R), Slave address can be set.
- External Hall sensor
- Self Auto-calibration with only one IIC command
- High speed non-volatile memory
  User free access : 96Byte
  Speed of write and read command (max) : 2.0MHz (IIC bus speed)
  EEPROM Store time (max) : 15ms
  EEPROM Read time : immediately
- PID controller
- Position command bit : 10bit resolution
- High accuracy position sensing.
- Rotation movement error cancelation.
- H bridged power out
- Power down mode
  (Mass Product only, ES sample does not support this function)
- Hall sensor position output : 10bit
- FRA (Frequency Response Analysis) Function is supported

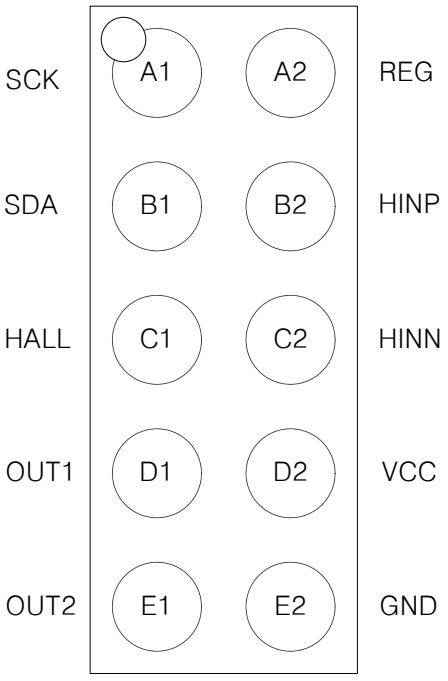
Application

- Mobile Magnetic application
- Camera phone

- Block Diagram



Pin assignments



Bumps Top view

Pin description

Pin Name	Pin No.	I/O	Description
SCK	A1	I	Serial Clock for I2C Interface
REG	A2	I/O	Regulator.
SDA	B1	I/O	Serial Data for I2C Interface
HINP	B2	I	Hall amplifier non-inverting input
HALL	C1	O	Hall constant current output.
HINN	C2	I	Hall amplifier inverting input.
OUT1	D1	O	Actuator Driver output1
VCC	D2	S	Power Supply
OUT2	E1	O	Actuator Driver output2
GND	E2	S	Ground

Maximum Absolute Rating

Parameter	Symbol	Value	unit
Supply Voltage	Vddmax	-0.3 ~ 4.0	V
Maximum Pin voltage (Normal)	Vpnmax	-0.3 ~ VDD+0.3	V
Maximum Pin voltage (Open Collector)	Vpomax	-0.3 ~ VDD+0.3	V
Storage temperature	Tstg	-40 ~ 150	℃
Operating temperature	Topr	-40 ~ 85	℃
Power Dissipation	Pdmax	800	mW

ESD Characteristics

Mode	Polarity	Characteristic			unit
		min	typ	max	
HBM	Positive/Negative	2000			V
MM	Positive/Negative	200			V
CDM	Positive/Negative	800			V

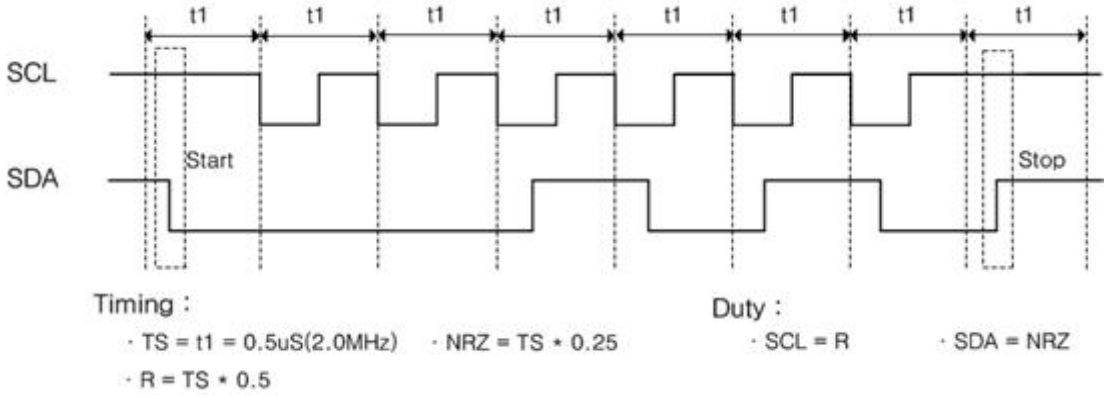
Electrical Characteristics

V = 1.8V to 3.6V, Ta=40~85℃ Unless otherwise noted

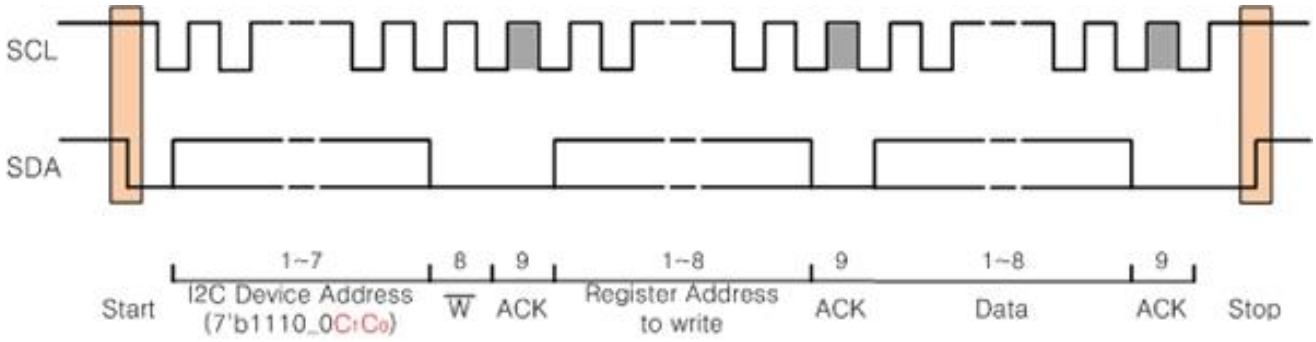
Characteristics	Symbol	Condition	Value			unit
			min	typ	max	
Operating supply voltage	Vcc	-	1.8	-	3.6	V
Self Auto calibration time	Tcal	-		400		ms
Current consumption	Icc1	Power down mode	-	-	2.0	uA*
	Icc2	Normal mode, No load, Vcc=2.8V	-	2.4	-	mA
	Icc3	High accuracy mode, No load, Vcc=2.8V	-	3.6	-	mA
	Icc4	Normal mode, No load, Vcc=3.3V	-	2.7	-	mA
	Icc5	High accuracy mode, No load, Vcc=3.3V	-	3.9	-	mA
Start (Ready) time	Ts	After Enable	-	-	1.0	mS
Output load	Rl	-	15	-	-	Ω
Output current	Iout	Rl=22ohm	-	100	-	mA
Logic input low voltage	Vthl	-	0	-	0.4	V
Logic input high voltage	Vthh	-	1.2	-	Vcc	V
EEPROM						
Memory write speed	fw	Write only	-	-	2.0	MHz
Memory read speed	fr	Read only	-	-	2.0	MHz
Memory store complete time	Ts	-	-	-	28	mS
EEPRom Endurance	EEN1	Ta=25℃	100K			cycle
	EEN2	Ta=125℃	10K			cycle
EEPRom Data retention	ERE	-	10			year

I2C Bus

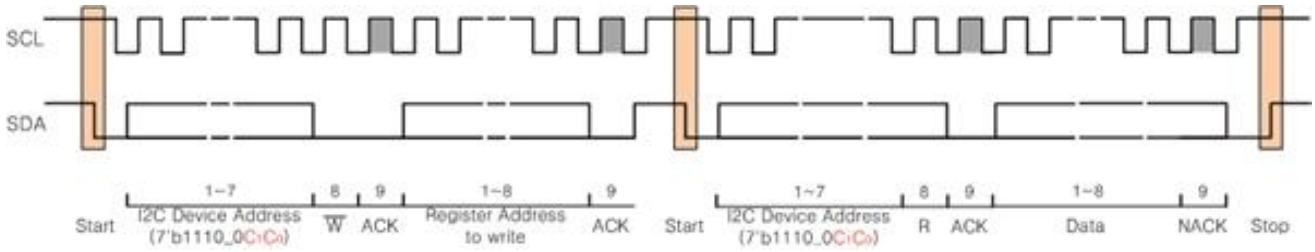
- I2C Timing (SCL, SDA)



- The timing flow of write mode is same below figure.



- The timing flow of read mode is same below figure.



Register Map

Address		R/W	Bit							
Register	EEPROM		7	6	5	4	3	2	1	0
–	0x00 ~ 0x5F	R/W	Customer free access area (96byte)							
0x90	0x60		O_drvpol	O_selpos	EVL	sysmd	O2_ackd		O2_dckd	
0x91	0x61		O6_gr						–	
0x92	0x62		EVL				CalLim[1:0]		O_selco[1:0]	
0x93	0x63		–			CalD1				
0x94	0x64		CalD2							
0x95	0x65		CalD3							
0x96	0x66		CalD4L		adjD1					
0x97	0x67		CalD4M		adjD2					
0x98	0x68		–		adjD3					
0x99	0x69		–		adjD4					
0x9A	0x6A		CalD5L							
0x9B	0x6B		–						CalD5M	
0x9C	0x6C		–						CB[1:0]	
0x9D	0x6D		Calconf		ADClpf		CalC			
–	0x6E ~ 0x7D		System Coefficient Area (16Byte)							
–	0x7E ~ 0x7F		–							
0x80		R/W	EVL			O_srst	OprMD[1:0]		O_drven	O_en
0x81			PosReg[7:0]							
0x82			CalMD	–	EVL	FRA_en	PosReg[11:8]			
0x83			EVL							
0x84		R	ADC[7:0]							
0x85			–		EEbusy	VMCS	ADC[11:8]			
0x86		R/W	Dinfra[7:0]							

: Reserved register

: Device supplier evaluation, setting or device Self generating area

: Module manufacturer setting area with/without device supplier assistance

: Customer control area

: Customer free usable area

-	0x00 ~ 0x5F	R/W	Customer free access area (96byte)

- Customer useable area(96Bytes)

0x90	0x60	R/W	O_drvpol	O_selpos	EVL	sysmd	O2_ackd	O2_dckd

- o_drvpol : Driving polarity selection register

o_drvpol	Direction
1'b0	Positive
1'b1	Negative

- o_selPos : Position Data Format selection register

o_drvopt	Mode
1'b0	10.0 Format
1'b1	10.2 Format

- EVL : This register is useable for IC debugging
  Customer should not access this register for normal operation

- sysmd : This register is useable for IC debugging
  Customer should not access this register for normal operation

- o2_ackd : Analog to digital converter clock frequency selection register

o2_ackd[1]	o2_ackd[0]	Clock frequency
0	0	Divide by 1 (24MHz)
0	1	Divide by 2 (12MHz)
1	0	Divide by 4 (6MHz)
1	1	Divide by 8 (3MHz)

- o2_dckd : Digital clock frequency selection register

o2_Dckd[1]	o2_Dckd[0]	Clock frequency
0	0	Divide by 1 (24MHz)
0	1	Divide by 2 (12MHz)
1	0	Divide by 4 (6MHz)
1	1	Divide by 8 (3MHz)

0x91	0x61	R/W	O6_gr	-

- o6_gr : Gain of Pre-amp selection register

O6_gr	Gain
63~0	X70 ~ X6 (1/step)

0x92	0x62	R/W	EVL	CalLim[1:0]	O_selco[1:0]

- EVL : This register is useable for IC debugging
  Customer should not access this register for normal operation

- CalLim : ADC noise cover range selection register on calibration
  ADC output data is change minutely, in spite of equivalent input when calibration.

calLim[1]	calLim[0]	Range
0	0	±1LSB
0	1	±2LSB
1	0	±4LSB
1	1	±8LSB

- o_selco[1:0] : Coefficients Changing range register
  PID coefficients can be changed automatically to improve performance about overshoot and response when gap of ADC and posReg is less than set-up value.

o_selco[1]	o_selco[0]	Range
0	0	±0LSB
0	1	±4LSB
1	0	±8LSB
1	1	±12LSB

0x93	0x63	R/W	-	CalD1

- CalD1 : Pre-amp input offset calibration data
  Value of CalD1 is determined by module calibration operation or Manual write enable.

0x94	0x64		CalD2

- CalD2 : Module calibration data2
  Input Current of hall is adjusted in value of CalD2
  Value of CalD2 is determined by module calibration operation or Manual write enable.

0x95	0x65	R/W	CalD3

- CalD3 : Module calibration data3
  Reference voltage of ADC is adjusted in value of CalD3
  Value of CalD3 is determined by module calibration operation or Manual write enable.

0x96	0x66	R/W	CalD4L	adjD1

- CalD4L : Module calibration LSB data4
  Input Current of hall is adjusted in value of CalD4
  Value of CalD4 is determined by module calibration operation or Manual write enable.

- adjD1 : Band-Gap Voltage adjustment register (Manufacturer adjustment)

0x97	0x67	R/W	CalD4M	adjD2

- CalD4M : Module calibration MSB data4
  Input Current of hall is adjusted in value of CalD4
  Value of CalD4 is determined by module calibration operation or Manual write enable.

- adjD2 : OSC frequency adjustment register (Manufacturer adjustment)

0x98	0x68	R/W	-	adjD3

- adjD3 : Hall Sensor Temperature adjustment register (Manufacturer adjustment)

0x99	0x69	R/W	-	adjD4

- adjD4 : Temperature Gain of Hall Sensor selection register (Manufacturer adjustment)

0x9A	0x6A	R/W	CalD5L	
0x9B	0x6B		-	CalD5M

- calD5 : This register is used for rotation error(temperature compensation) correction.

0x9C	0x6C	R/W	-	CB[1:0]

- CB : I2C custom bit register

CB[1]	CB[0]	Slave Address(W/R)
0	0	0xE0 / 0xE1
0	1	0xE2 / 0xE3
1	0	0xE4 / 0xE5
1	1	0xE6 / 0xE7

0x9D	0x6D	R/W	Calconf	ADClpf	CalC

- Calconf : Calibration configuration, Use manufacturer recommended value.(2'b11)

- ADClpf : ADC filter configure register

ADClpf[1]	ADClpf[0]	Cutoff Frequency
0	0	0.9KHz @24MHz
0	1	1.8KHz @24MHz
1	0	3.6KHz @24MHz
1	1	Bypass

- CalC : Calibration error flag register

  CalC[3] : Pre-amp offset calibration error register

  CalC[2] : Hall offset calibration error register 1 *

  CalC[1] : Hall gain calibration error register

  CalC[0] : Hall offset calibration error register 2 *

  If calibration operation is operated abnormally, this bits are will be set.

  * Hall offset operation is implemented twice for enhancing accuracy

-	0x6E ~ 0x7D	R/W	System Coefficient Area (16Byte)

- System Coefficient area : This registers are used for PID controller

0x80		R/W	EVL	O_srst	OprMD[1:0]	O_drven	O_en

- EVL : This register is useable for IC debugging

  Customer should not access to this register for normal operation

- o_srst : Software Reset

  When this register is high status, all blocks reset and then it will be clear automatically

- OprMD : Operation accuracy selection register

  This register is used to select VMCS range, (Actuator movement OK signal.)

oprMD[1]	oprMD[0]	Range
0	0	±1LSB
0	1	±2LSB
1	0	±3LSB
1	1	±4LSB

- o_drven : Output Driver Enable register

When this register is set, output driver is enabled

- o_en : Analog block Enable register(Reference block, OSC, ADC, etc..)
  When this register is set, analog block is enabled

0x81		R/W	PosReg[7:0]				
0x82			CalMD	-	EVL	FRA_en	PosReg[11:8]

- PosReg : 12-bit target position register

- CalMD : Calibration operation start register
  When this register is set, calibration is implemented
  This register is clear automatically after calibration completion

- EVL : This register is useable for IC debugging
  Customer should not access to this register for normal operation

- FRAen : Frequency Response Analysis enable.
  If this register is set,
  Main feedback will be off, and the H bridge output is controlled by Dinfra value

0x83		R/W	EVL

- EVL : This register is useable for IC debugging
  Customer should not access to this register for normal operation

0x84		R	ADC[7:0]			
0x85			-	EEbusy	VMCS	ADC[11:8]

- ADC : ADC output register
- EEbusy : EEProm Busy register
  When this register is low status, you shouldn't access into EEProm
- VMCS : Actuator movement completion register
  This registers are read only
  even if this register is high, the PID feedback operation is ongoing.

0x86		R/W	Dinfra[7:0]

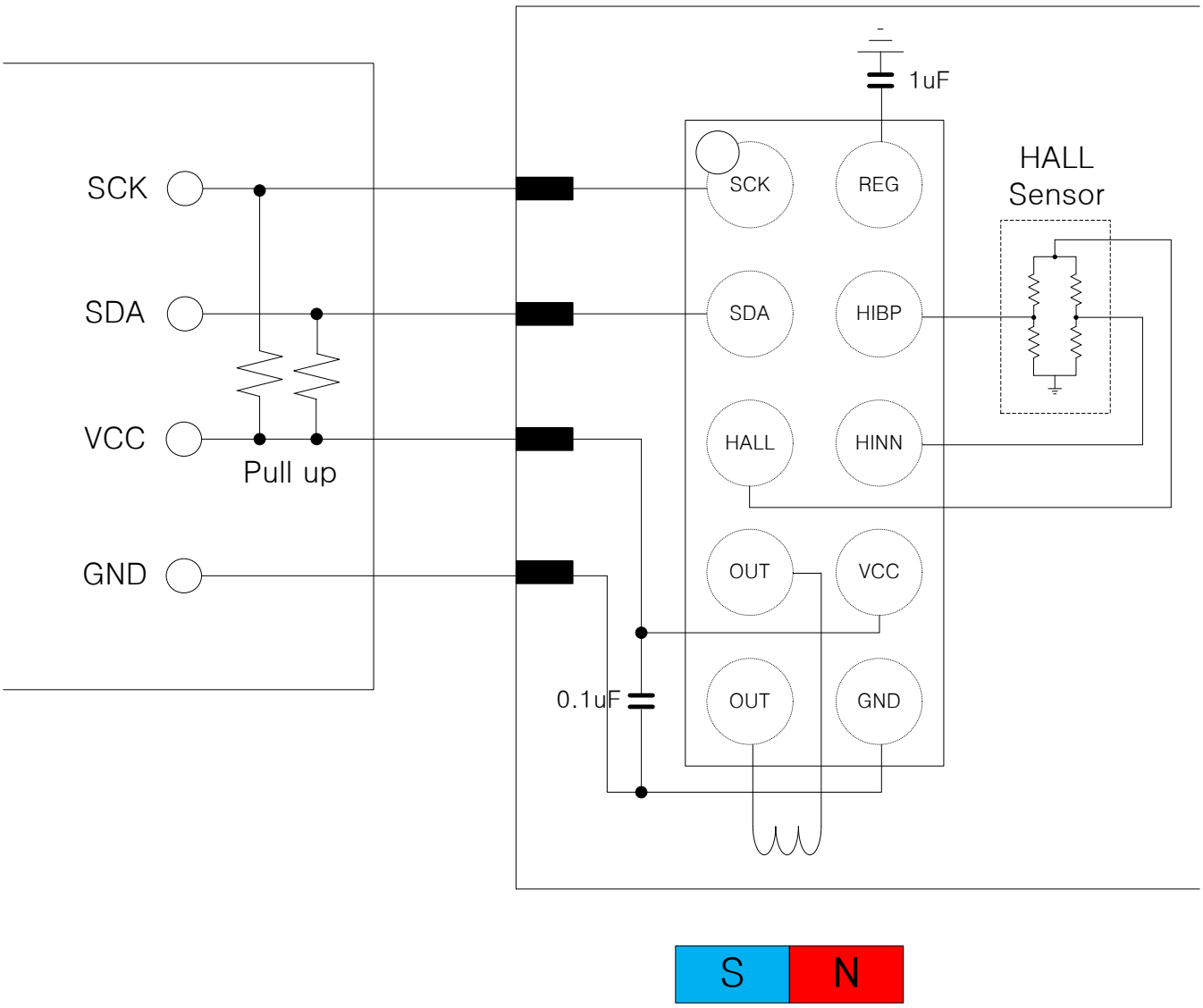
- Dinfra : Output data register when FRA_en is set.
  The output voltage is determined by this register value.

Frequency Response Analysis

This option is for measuring module`s frequency response.
If FRAen(0x82[4]) is set, this option should be enable.

You can control driving power to change Dinfra(0x86) value.
According to changing of input frequency(Dinfra),
you can monitor continuously changed ADC value(0x84&0x85) that represents module`s position.
You can estimate module`s frequency response, as you analyze ADC value.

Application Circuit



FRA (Frequency Response Analysis) Circuit