NEXT Lab

Semiconductor Development Group

NXM5004

OIS Control Driver & 8MByte EEPROM

General Description

The NXM5004 is an image stabilization system controller for Smartphone camera module.

This controller has built-in PID controller, 2ch H-Bridge Driver for VCM type actuators, 12bit ADC and 4ch. 8bit DAC.

This controller can detect temperature change for compensation of the external hall.

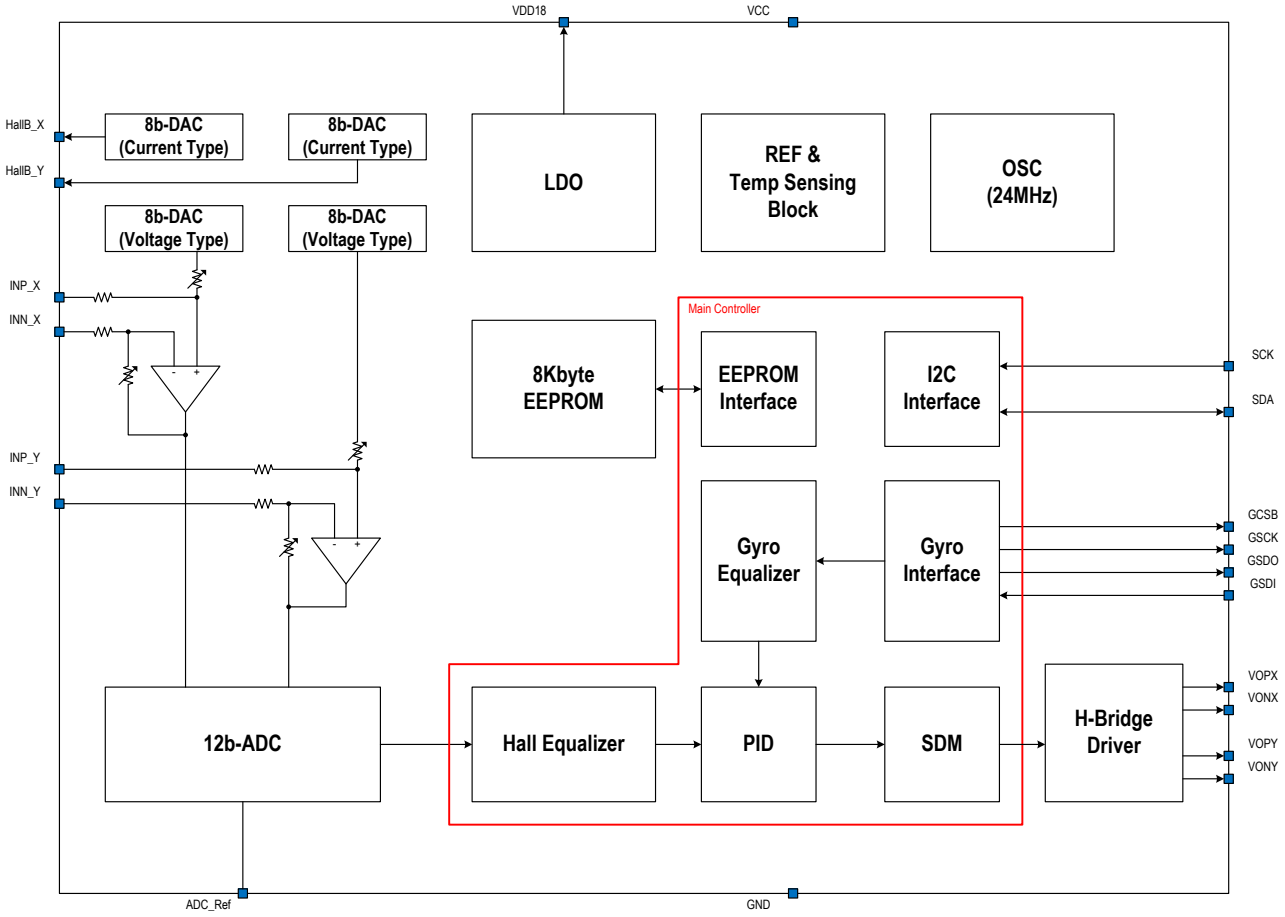
Feature

- Supply voltage : 2.4V ~ 3.6V.
- IIC Interface : Standard / Fast mode (Max 2.0Mhz supported)
  Default Slave address 0xE0/0xE1(W/R), Slave address can be changed by set-up.
- Self Auto-Calibration with only one IIC command.
- High speed non-volatile memory.
  Speed of write and read command (max) : 2.0MHz (IIC Bus speed).
  EEPROM Store time (max) : 15ms.
  EEPROM Read time : immediately.
- High resolution PID controller.
- Built-in 2ch. Current Drive DAC and 2ch. Voltage Drive DAC for calibration.
- Built-in 1ch. 12bit ADC.
- Built-in LDO.
- Built-in OSC (24MHz ±3%, Frequency adjustment function).
- Compensation variation of hall for temperature.
- Digital Gyro I/F for the companies (SPI Bus).
- FRA (Frequency Response Analysis) Function is supported.
- Package : Not Determined.

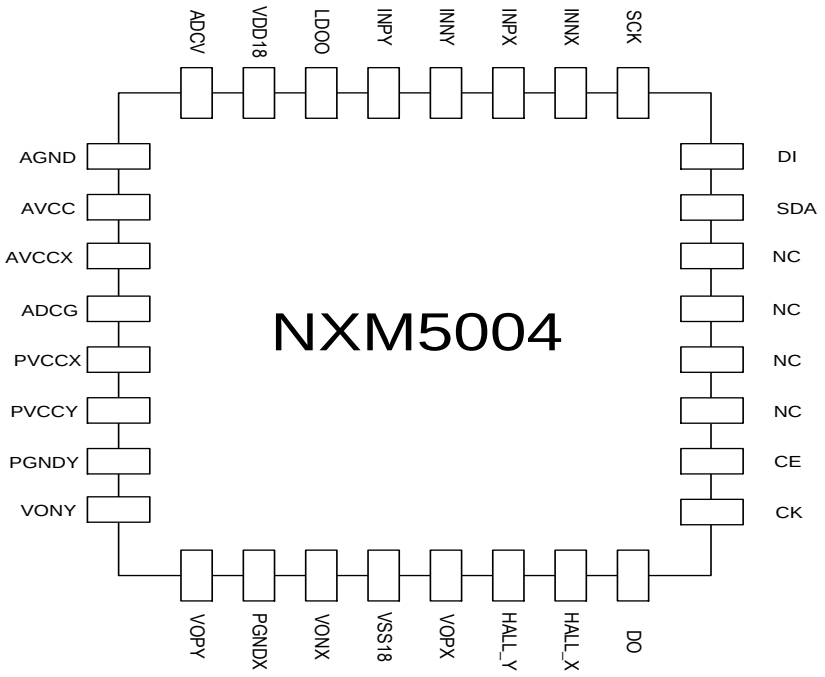
Application

- Smartphone Camera Module application.

Block Diagram



Terminal assignment (32Pin QFN)



Pin Description

Pin No	Pin Name	Function
1	AGND	Analog GND
2	AVCC	Analog VCC
3	AVCCX	Analog VCC
4	ADCG	ADC GND
5	PVCCX	X - Channel Power VCC
6	PVCCY	Y - Channel Power VCC
7	PGNDY	Y – Channel Power GND
8	VONY	Y – Channel Negative Drive Output
9	VOPY	Y – Channel Positive Drive Output
10	PGNDX	X – Channel Power GND
11	VONX	X – Channel Negative Drive Output
12	VSS18	GND
13	VOPX	X – Channel Positive Drive Output
14	HALL_Y	Y-CH Hall Bias
15	HALL_X	X-CH Hall Bias
16	DO	SDI(Output) for Gyro Interface
17	CK	SCK for Gyro Interface
18	CE	CSB for Gyro Interface
19	NC	-
20	NC	-
21	NC	-
22	NC	-
23	SDA	SDA for I2C Interface
24	DI	GSDO(Input) for Gyro Interface
25	SCK	SCK for I2C Interface
26	INNX	X-CH Hall Amplifier Negative Input
27	INPX	X-CH Hall Amplifier Positive Input
28	INNY	Y-CH Hall Amplifier Negative Input
29	INPY	Y-CH Hall Amplifier Positive Input
30	LDOO	1.8V LDO Output
31	VDD18	1.8V Input
32	ADCV	ADC Reference Voltage Output

Electrical Characteristics

V = 1.8V to 3.6V, Ta =40~85℃ Unless otherwise noted

Characteristics	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Operating supply Voltage	Vcc	-	1.8V	-	3.6V	V
Self Auto calibration time	Tcal	-		700		ms
Current consumption	Icc1	Power down mode			2.0	uA
	Icc2	Normal mode No load, Vcc = 2.8V		7.6		mA
	Icc3	Normal mode No load, Vcc = 3.3V		7.7		mA
Start (Ready) time	Ts	After Enable			1.0	ms
Output Load	RI	-	15			Ω
Output current	Iout	RI=22ohm		100		mA
Logic input low voltage	Vthl	-	0		0.4	V
Logic input high voltage	Vthh	-	1.2		Vcc	V
EEPROM						
Memory Write Speed	Fw	Write only			2.0	Mhz
Memory Read Speed	Fr	Read only			2.0	Mhz
Memory store complete time	Ts	-	-	-	28	ms
EEPROM Endurance	EEN1	Ta=25℃	100K			Cycle
	EEN2	Ta=125℃	10K			Cycle
EEPROM Data retention	ERE	-	10			year

Maximum Absolute Rating

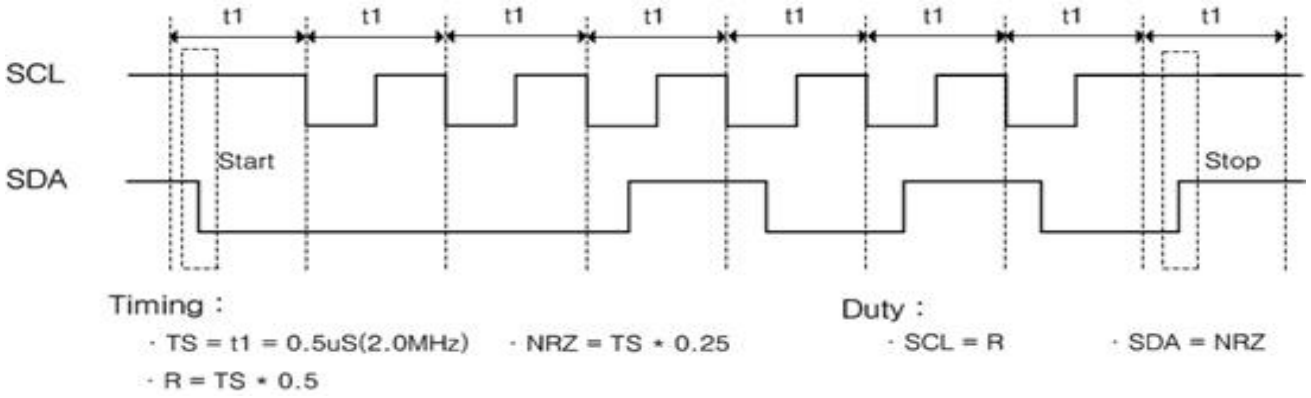
Parameter	Symbol	Value	unit
Supply Voltage	Vddmax	-0.3 ~ 4.0	V
Maximum Pin voltage (Normal)	Vpnmax	-0.3 ~ VDD+0.3	V
Maximum Pin voltage (Open Collector)	Vpomax	-0.3 ~ VDD+0.3	V
Storage temperature	Tstg	-40 ~ 150	℃
Operating temperature	Topr	-40 ~ 85	℃
Power Dissipation	Pdmax	800	mW

ESD Characteristics

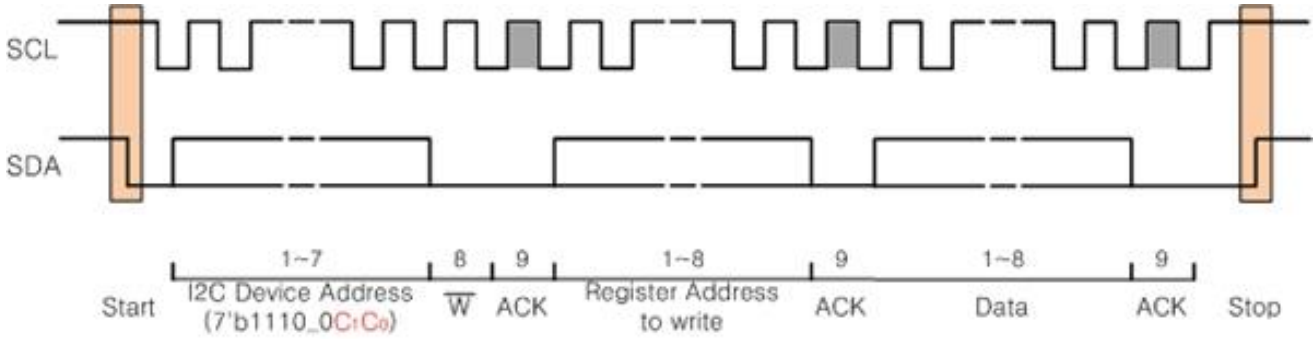
Mode	Polarity	Characteristic			unit
		min	typ	max	
HBM	Positive/Negative	4000			V
MM	Positive/Negative	200			V
CDM	Positive/Negative	800			V

I2C Bus Interface

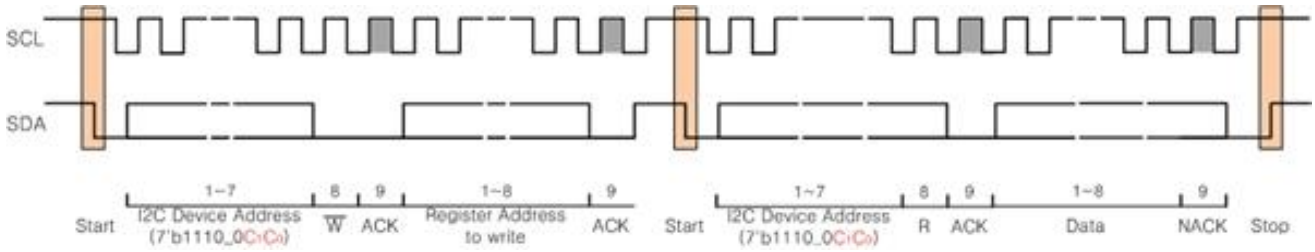
- **I2C Timing (SCL, SDA)**



- **The timing flow of write mode is same below a figure.**



- **The timing flow of read mode is same below a figure.**



Register Map

Address	R/W	Bit							
Register		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x00 ~0x1F	R/W	EEPROM AREA							
0x20		O_srst	Opofctrl	GyroWR	GyroRD	OprMD[1:0]		O_DRVEN	O_EN
0x21		CalMD	-				FraMD	FRA_enX	FRA_enY
0x22		Ften	-			O_TESTEN	O3_TESTADD		
0x23		DinfraX[7:0]							
0x24		DinfraY[7:0]							
0x25		GyroAdd[7:0]							
0x26		GyroWData[7:0]							
0x27		-				TEST[1:0]		REG7	REG0
0x28		MemSel[7:0]							
0x29	R	GyroRData1[7:0]							
0x2A		GyroRData2[7:0]							
0x2B		ADCX[7:0]							
0x2C		-		EEPbusy	VMCSX	ADCX[11:8]			
0x2D		ADCY[7:0]							
0x2E		-			VMCSY	ADCY[11:8]			
0x2F		ADCTemp[11:4]							
0x30		Gyro Word 1[7:0]							
0x31		Gyro Word 1[15:8]							
0x32		Gyro Word 2[7:0]							
0x33		Gyro Word 2[15:8]							
0x34		Gyro Word 3[7:0]							
0x35		Gyro Word 3[15:8]							
0x36		Gyro Word 4[7:0]							
0x37		Gyro Word 4[15:8]							
0x80	R/W	DrvpolX	DrvpolY	TconEN	-			ckDiv[1:0]	
0x81		o8_r2X							
0x82		o8_r2Y							
0x83		OpenI2C	DrvDir	selCo[1:0]		CalLim[1:0]		CalPow[1:0]	
0x84		selSameNu	selDivEoc	-	DisRange[2:0]			selLpfAdc[1:0]	
0x85		InDisRate[1:0]		PreHPF[2:0]			PostHPF[2:0]		
0x86		GyroGainX[7:0]							
0x87		GyroGainY[7:0]							
0x88		GyroGainY[11:8]				GyroGainX[11:8]			
0x89		o_Bon	o_TsdEN	o6_Tsdata[5:0]					
0x8A		ADCompX[7:0]							
0x8B		ADCompY[7:0]							

Address	R/W	Bit							
Register		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
0x8C	R/W	Hcoeff							
0x8D		-		o6_bgd					
0x8E		-		o6_tsd					
0x8F		-		o6_dac0					
0x90		-		o6_oscd					
0x91		-						CB[1:0]	
0x92		-			o5_opcalX				
0x93		o8_dac1X							
0x94		o8_dac2X							
0x95		-			o5_opcalY				
0x96		O8_dac1Y							
0x97		O8_dac2Y							
0x98		ADCtcal[7:0]							
0x99		Pre_ampY	Offset1Y	GainY	Offset2Y	Pre_ampX	Offset1X	GainX	Offset2X
0x9A ~0x9F		Not Determined							
0xA0 ~0xBF		System Coefficient Area X (16 Byte) System Area (2)							
		System Coefficient Area Y (16 Byte) System Area (2)							
0xC0 ~0xDF		Custom control byte for Gyro 1 (32 Byte) System Area (3)							
0xE0 ~0xFF		Custom control byte for Gyro 2 (32 byte) System Area (4)							

※ Register Default Value

Address 0x00 ~ 0x1F : EEPROM Data(0x0000 ~ 0x001F)

Address 0x20 ~ 0x37 : 0x00

Address 0x80 ~ 0xFF : EEPROM Data(0x1F80 ~ 0x1FFF)

: Reserved area

: Device supplier evaluation, setting or device Self generating area

: Module manufacturer setting area with/without device supplier assistance

: Customer control area

: Customer free usable area

Register Map Description

Reg Add	Reg Name	Description
0x00 ~0x1F	EEPROM	32 Bytes EEPROM Area
0x20[0]	o_EN	Analog Enable (0) Disable (1) Enable
0x20[1]	o_DRVEN	Output Driver Enable (0) Disable (1) Enable
0x20[3:2]	OprMD[1:0]	Operation Mode (0) ±1 (1) ±2 (2) ±3 (3) ±4
0x20[4]	GyroRD	Gyro Read Command Start
0x20[5]	GyroWR	Gyro Write Command Start
0x20[6]	Opofctrl	Op-Amp Offset Cal Control (0) Low (1) High When Opofctrl bit is “High”, two amp input short
0x20[7]	o_srst	Software Reset (0) Normal operation (1) Reset
0x21[0]	FRA_enY	Y channel FRA Enable (0) Disable (1) Enable
0x21[1]	FRA_enX	X channel FRA Enable (0) Disable (1) Enable
0x21[2]	FraMD	FRA mode (0) Direct PWM (1) PID PWM
0x21[7]	CalMD	Auto Calibration Enable (0) Disable (1) Enable
0x22[2:0]	o3_TESTADD[2:0]	Test Output Address (Number 0 ~ 7)
0x22[3]	o_TESTEN	Test Enable (0) Disable (1) Enable
0x22[6:4]	NDADDR[2:0]	Node Probe Address (Number 0 ~ 7)
0x22[7]	Ften	CheckSum Test Enable (0) Disable (1) Enable
0x23[7:0]	DinfraX[7:0]	X-channel FRA data (Default :0x80)
0x24[7:0]	DinfraY[7:0]	Y-channel FRA data (Default : 0x80)
0x25[7:0]	GyroAdd[7:0]	Gyro SPI Sub Address
0x26[7:0]	GyroWData[7:0]	Gyro SPI Write Data
0x27[0]	REG0	Flash Input REGDATA[0]
0x27[1]	REG7	Flash Input REGDATA[7]
0x27[3:2]	TEST[1:0]	Flash Input TEST[1:0]
0x27[7:4]	Reserved Reg	Reserved Register
0x28[7:0]	MemSel[7:0]	EEPROM Assign Resigter -> ADD256(32BYTE)
0x29[7:0]	GyroRData1[7:0]	Gyro Read Data1
0x2A[7:0]	GyroRData2[7:0]	Gyro Read Data2
0x2C[3:0] &0x2B[7:0]	ADCX[11:0]	X – channel ADC output register

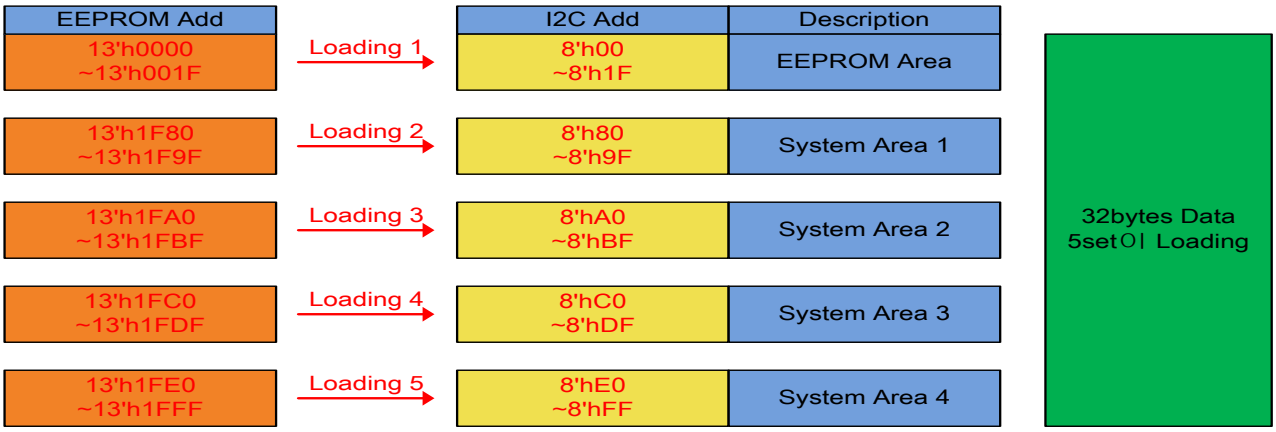
Reg Add	Reg Name	Description
0x2C[4]	VMCSX	X – Channel Movement Complete Signal
0x2C[5]	EEPbusy	EEPROM Busy Signal
0x2E[3:0] ~0x2D[7:0]	ADCY[11:0]	Y – Channel ADC output register
0x2E[4]	VMCSY	Y – Channel movement Complete Signal
0x2F[7:0]	ADCTemp[11:4]	Temp Bias ADC output (MSB 8bit)
0x30[7:0]	GyroWord1[7:0]	Gyro Read Word 1 (LSB 8bit)
0x31[7:0]	GyroWord1[15:8]	Gyro Read Word 1 (MSB 8bit)
0x32[7:0]	GyroWord2[7:0]	Gyro Read Word 2 (LSB 8bit)
0x33[7:0]	GyroWord2[15:8]	Gyro Read Word 2 (MSB 8bit)
0x34[7:0]	GyroWord3[7:0]	Gyro Read Word 3 (LSB 8bit)
0x35[7:0]	GyroWord3[15:8]	Gyro Read Word 3 (MSB 8bit)
0x36[7:0]	GyroWord4[7:0]	Gyro Read Word 4 (LSB 8bit)
0x37[7:0]	GyroWord4[15:8]	Gyro Read Word 4 (MSB 8bit)
0x80[1:0]	ckDiv[1:0]	Clock Divider (0) 1Div (1) 2Div (2) 4Div (3) 8Div
0x80[5]	TconEN	Temp Compensation Enable (0) Disable (1) Enable
0x80[6]	DrvpolY	Y – Channel Drive Polarity Selection
0x80[7]	DrvpolX	X – Channel Drive Polarity Selection
0x81[7:0]	o8_r2X	X-Channel Op-Amp Gain Selection
0x82[7:0]	o8_r2Y	Y-Channel Op-Amp Gain Selection
0x83[1:0]	CalPow[1:0]	Calibration Power Selection
0x83[3:2]	CalLim[1:0]	Calibration Error Limit Selection (0) ±1 (1) ±2 (2) ±3 (3) ±4
0x83[5:4]	selCo[1:0]	Coeff Change Range Selection (0) ±0 (1) ±4 (2) ±8 (3) ±12
0x83[6]	DrvDir	Open Loop Drive Direction Selection
0x83[7]	OpenI2C	Open Loop Drive Mode Enable (0) Disable (1) Enable
0x84[1:0]	selLpfAdc[1:0]	ADC Output LPF (Average) (0) 0.5 khz (1) 1khz (2) 2khz (3) bypass
0x84[4:2]	DisRange[2:0]	PID intergrator Discharge Range (0) Discharge Off (1) less than 2% (2) less than 4% (3) less than 6% (4) less than 8% (5) less than 10% (6) less than 12% (7) always Discharge On
0x84[6]	selDivEoc	Calibration count number for judgment (0) 32 (1) 62

0x84[7]	selSameNum	Calibration cycle for judgment (0) 8 div (1) 16 div
0x85[2:0]	PostHPF[2:0]	Post High Pass Filter Pole Selection for Gyro Data (0) 0.1hz (1) 0.05hz (2) 0.0334hz (3) 0.025hz (4) 0.002hz (5) 0.0167hz (6) 0.0143hz (7) 0.0125hz
0x85[5:3]	PreHPF[2:0]	Pre High Pass Filter Pole Selection for Gyro Data (same value PostHPF)
0x85[7:6]	IntDisRate[1:0]	Intergrator Discharge Rate (0) 2.5s (1) 5s (2) 10s (3) 20s
0x86[7:0] 0x88[3:0]	GyrogainX[11:0]	X – channel Gyro Gain (-2.0 ~~ +2.0) MSB : Signed bit, 1.10bit format
0x87[7:0] 0x88[7:4]	GyrogainY[11:0]	Y – channel Gyro Gain (-2.0 ~~ +2.0) MSB : Signed bit, 1.10bit format
0x89[5:0]	o6_Tsdata[5:0]	Thermal Shut Down adjust data
0x89[6]	o_TsdEN	Thermal Shut Down Enable (0) Disable (1) Enable
0x89[7]	o_Bon	ADC Boost option Enable (0) Disable (1) Enable
0x8A[7:0]	ADCompX[7:0]	X – channel ADC compensation Register
0x8B[7:0]	ADCompY[7:0]	Y – channel ADC compensation Register
0x8C[7:0]	Hcoeff	Temp,Parameter (signed 1bit, 0.7bit, Hall coeff)
0x8D[5:0]	o6_bgd	Band Gap Adjust Data
0x8E[5:0]	o6_tsd	Temp Coeff Adjust Data
0x8F[5:0]	o6_dac0	DAC1 Reference Current Adjust data
0x90[5:0]	o6_oscd	Internal OSC Adjust Data
0x91[1:0]	CB[1:0]	I2C Custom Bit
0x92[7:0]	o5_opcalX	X – channel Amp Offset Cal Data
0x93[7:0]	o8_dac1X	X – channel Hall Gain Cal Data
0x94[4:0]	o8_dac2X	X – channel Reference Voltage of ADC Cal Data
0x95[7:0]	o5_opcalY	Y – channel Amp Offset Cal Data
0x96[7:0]	o8_dac1Y	Y – channel Hall Gain Cal Data
0x97[7:0]	o8_dac2Y	Y – channel Reference Voltage of ADC Cal Data
0x98[7:0]	ADCtcal[7:0]	In state of Calibration , output ADC of bandgap bias
0x99[7:0]		Each of X , Y channel Error Bit Offset2 error , Gain error, Offset1 error, Pre-amp error

EEPROM Loading

MemSel[7:0]	I2C register	EEPROM ADD 13b	Description	Total
0x00~0xFB	0x00~0x1F	13'h0000~13'h1F7F	User Area(7K+896) bytes	8K bytes (Write Max 32Bytes)
0xFC	0x00~0x1F	13'h1F80~13'h1F9F	System Area(1) 32 Bytes	
0xFD	0x00~0x1F	13'h1FA0~13'h1FBF	System Area(2) 32 Bytes	
0xFE	0x00~0x1F	13'h1FC0~13'h1FDF	System Area(3) 32 Bytes	
0xFF	0x00~0x1F	13'h1FE0~13'h1FFF	System Area(4) 32 Bytes	

1) If chip Enable, data in EEPROM are loaded into System Register as shown below picture



2) EEPROM Read

If the value of Memsel is Update, EEPROM data corresponding to the value of Memsel is loaded to I2C address from 0x00 to 0x1F and read the I2C address.

3) EEPROM Write

Access to I2C Address from 0x00 to 0x1F, and write data. After I2C Communication END, I2C Register Data is written to EEPROM Add according to the value of MemSel.

(It is possible to write up to 32 Bytes)

Gyro Interface Register

Name	I2C Add	Description
WriteComm[0] ~ WriteComm[25]	0xC0~0xF3 (2bytes X 26ea)	Write Command 26ea
GSlpComm	0xF4 & 0xF5 (2bytes)	Gyro SLP Command
ReadComm[0]	0xF6(1byte)	Read Command 4ea
ReadComm[1]	0xF7(1byte)	
ReadComm[2]	0xF8(1byte)	
ReadComm[3]	0xF9(1byte)	
WriteNum[4:0]	0xFA[4:0]	Write Com Number
Reserved	0xFA[7:5]	Reserved Reg
ReadNum[1:0]	0xFB[1:0]	Read Com Number
RDataNum[2:0]	0xFB[4:2]	Read Data Number
Reserved	0xFB[7:5]	Reserved Reg
PolaritySCK	0xFC[0]	SCK Polarity Sel
Reserved	0xFC[3:1]	Reserved Reg
WSckSel[1:0]	0xFC[5:4]	Write SCK Frequency Select
RSckSel[1:0]	0xFC[7:6]	Read SCK Frequency Select
DLengthH[2:0]	0xFD[2:0]	High Data Length
DLengthL[2:0]	0xFD[5:3]	Low Data Length
HighSel	0xFD[6]	High Byte Selection
CsbSel	0xFD[7]	CSB Active Select
SMsbH[2:0]	0xFE[2:0]	High MSB Start Bit
SmsbL[2:0]	0xFE[5:3]	Low MSB Start Bit
BitDir	0xFE[6:0]	Bit Direction Selection
SignedBit	0xFE[7]	Signed Bit Selection
Reserved	0xFF[7:0]	Reserved Register

Gyro Interface Register Description

- Write Comm
  gyro write command
  it is consist of 2 byte.(sub address + data)
  it makes maximum 32 command

- GSlpComm
  When chip Disable, external gyro chip Disable

- ReadComm
  Gyro Read command
  It makes Maximum 4 command

- WriteNum
  Setting the number of write command
  Write Number = WriteNum + 1

- ReadNum
  Setting the number of read command
  Read Number = ReadNum + 1

- RDataNum
  Setting the number of Read Data per 1 Read Command
  Data Number = RDataNum + 1

- PolaritySCK
  Setting Polarity SCK

- WSckSel
  Setting SCK frequency in Write Mode and Read Mode

WSckSel=0 RSckSel=0	WSckSel=1 RSckSel=1	WSckSel=2 RSckSel=2	WSckSel=3 RSckSel=3
1Mhz	0.8Mhz	0.6Mhz	0.4Mhz

- DLengthH & DLengthL
  Setting High Data Length and Low Data Length

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
DLengthH=7	DLengthH=6	DLengthH=5	DLengthH=4	DLengthH=3	DLengthH=2	DLengthH=1	DLengthH=0
DLengthL=7	DLengthL=6	DLengthL=5	DLengthL=4	DLengthL=3	DLengthL=2	DLengthL=1	DLengthL=0

- HighSel
  Setting High Byte Selection

HighSel = 0		HighSel = 1	
ReadData1	ReadData2	ReadData1	ReadData2
High Byte[7:0]	Low Byte[7:0]	Low Byte[7:0]	High Byte[7:0]

- CsbSel
  Setting CSB Active Selection
  “High = active High” “Low = active Low”

- SMsbH & SMsbL
  Setting High MSB Start Bit and Low MSB Start Bit Selection

Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
SMsbH=0	SMsbH=1	SMsbH=2	SMsbH=3	SMsbH=4	SMsbH=5	SMsbH=6	SMsbH=7
SMsbL=0	SMsbL=1	SMsbL=2	SMsbL=3	SMsbL=4	SMsbL=5	SMsbL=6	SMsbL=7

- BitDir
  Setting Bit Direction Selection
  “High = Bit Moves from Right to Left” “Low = Bit Moves from Left to Right”

- SignedBit
  Setting Signed Bit Selection
  “High = Unsigned” “Low = Signed”

Frequency Response Analysis

This option is measuring Module’s frequency response.

Before measuring the FRA, Register Bit FRAenX(0x21[1]) or FRAenY(0x21[0]) is set High.

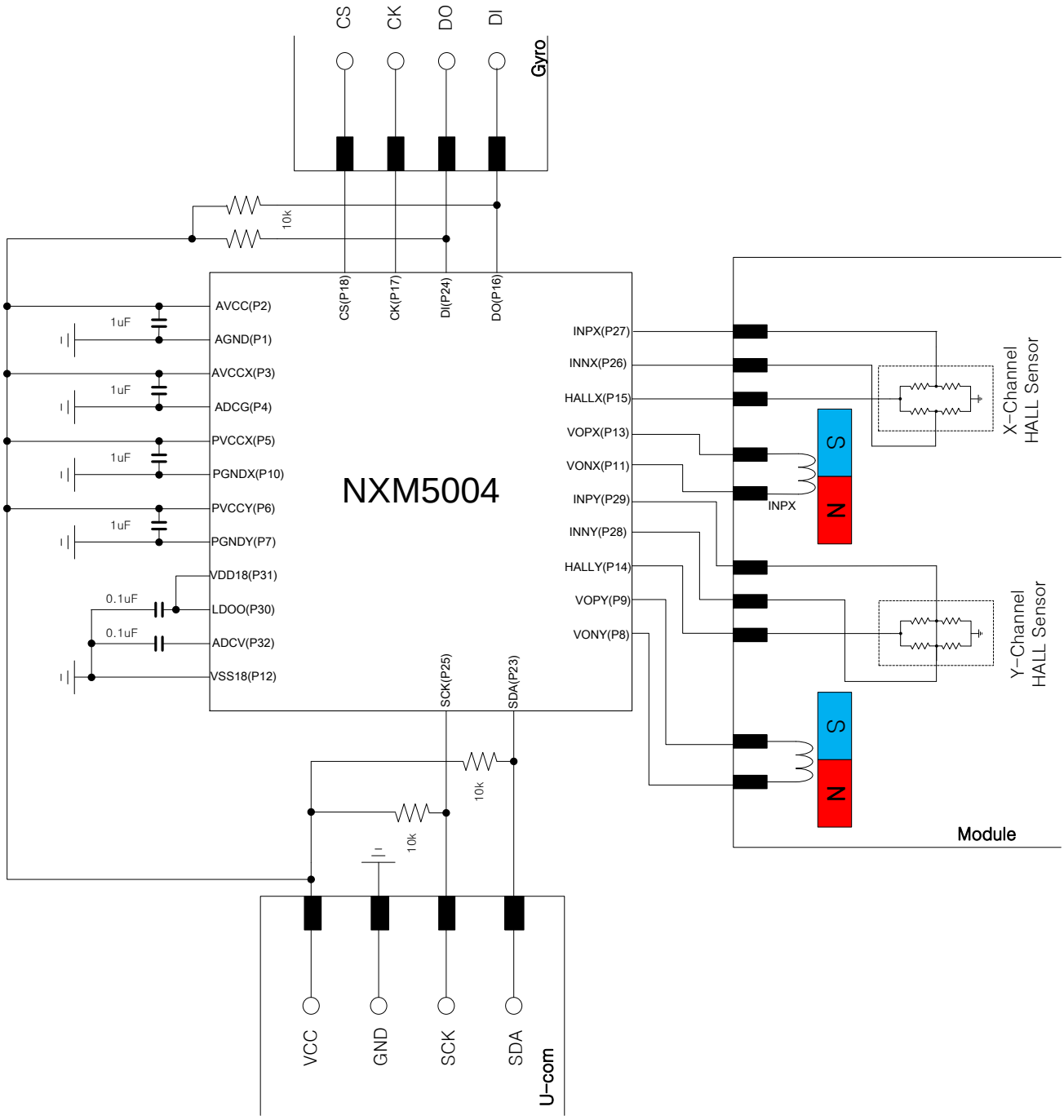
Register DinfraX(0x23) or DinfraY(0x24) can control driving power.

According to changing of input frequency(DinfraX/DinfraY),

Possible to monitor continuously changed ADCX(0x2B&0x2C) and ADCY(0x2D&0x2E) value that represent module’s position.

You can estimate module`s frequency response, as you analyze ADC value.

Application Circuit



Package Outline(Not determined)