NEXT Lab

Semiconductor Development Group

NXM5003

10bit Resolution VCM driver IC with I2C interface

General Description

The NXM5003 is single 10-bit decoder with 120mA output current sink capability.

It includes power-on reset circuit, power-down function, and exactly matched driver circuit.

The decoder is controlled via a I2C serial interface that operates decoder by clock rates up to 400kHz.

The NXM5003 is designed for auto focus and optical zoom camera phones, digital still cameras, and camcorders applications.

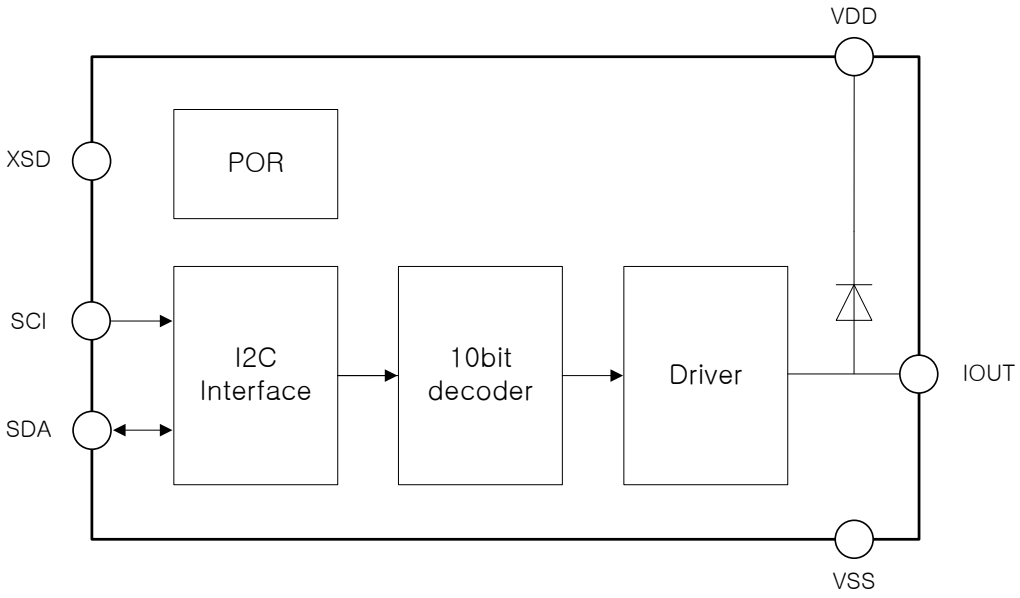
Feature

- Supply voltage : 2.3V ~ 3.6V
- VCM driver for auto-focus
- 10bit decoder
- 120mA output current sink capability
- VCM Smart Transition Control(STC)
- Fast mode I2C interface (1.8V interface available)
- Power on reset (POR)
- Package : 0.75mm(W) X 1.15mm(H) 6pin-WLP

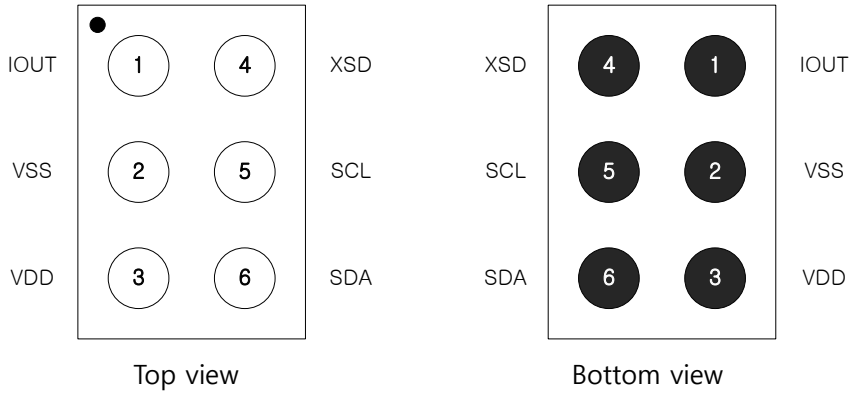
Application

- Digital camera
- Cell Phones
- Lens auto focus
- Web camera

Block Diagram



Pin assignments



Pin description

Pin Name	Pin No.	I/O	Description
IOUT	1	O	Output current sink
VSS	2		Ground
VDD	3		Power supply
SDA	4	I/O	Serial data
SCL	5	I	Serial Clock Line
XSD[(1)]	6	I	Shutdown mode (active low)

(1) XSD : Shutdown mode (active low)
1 : Normal operation mode
0 : Shutdown mode

Maximum Absolute Rating

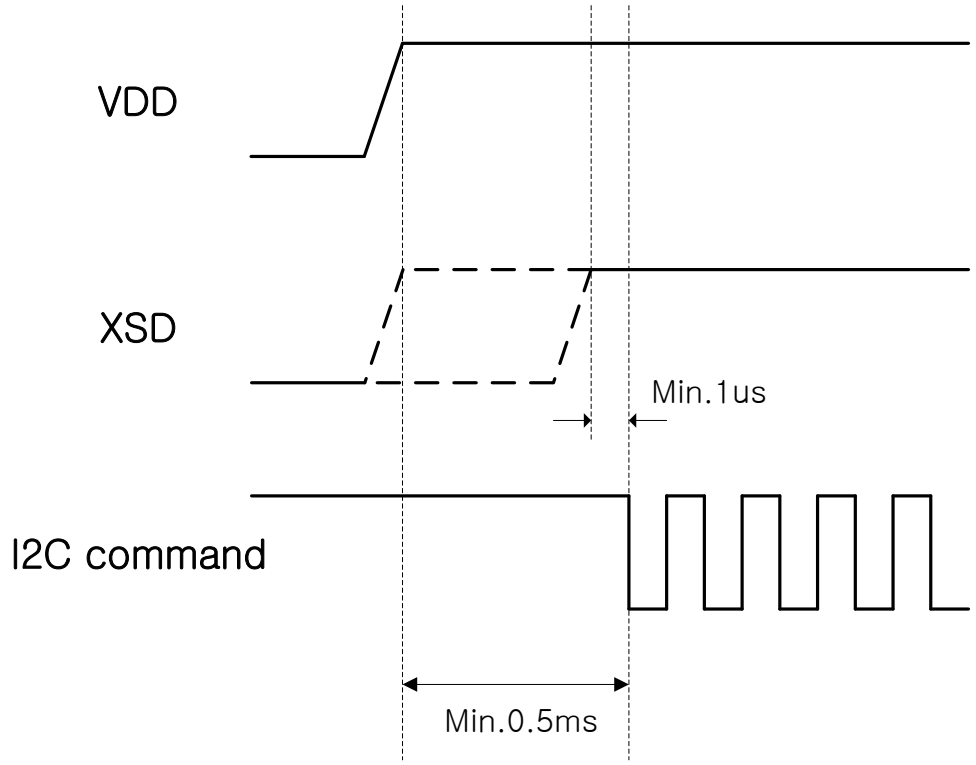
Parameter	Symbol	Value	unit
Supply Voltage	VDD	−0.3 ~ 4.5	V
Control input voltage	Vin	−0.3 ~ VDD+0.3	V
Human body model	Vhbm	2	KV
Machine model	Vmm	200	V
Operating temperature range	Topr	−40 ~ 85	℃
Junction temperature	Tj	150	℃

Electrical Characteristics

V = 2.3V to 3.6V, Vin = 1.8V to VDD, Ta=25℃ Unless otherwise noted

Characteristics	Symbol	Conditions	Min	Typ	Max	unit
Overall						
Input Voltage Range	VDD		2.3		3.6	V
Shutdown mode	ISD	XSD = Low			1	uA
Quiescent mode	IQ_1	XSD = High, PD = HIgh	0.24		0.35	mA
	IQ_2	Data = 0		0.5		mA
	IQ_3	Data = 1		0.62		mA
Logic input / output (XSD)						
Input current					1	uA
Low Level Input Voltage	VIL				0.54	V
High Level Input Voltage	VIH		1.26			V
Logic input / output (SCL, SDA)						
Input current					1	uA
Low Level Input Voltage	VIL				0.54	V
High Level Input Voltage	VIH		1.26			V
Low Level Output Voltage	VOL	I sourcing = 3mA(SDA)			0.4	V
Glitch rejection				50		ns
VCM driver						
Current resolution		117.34uA/LSB		10		Bits
INL	INL	VDD = 2.8V	−2		+2	LSB
DNL	DNL		−1		+1	LSB
Zero code error	ZCE	Zero data loaded to decoder			1	uA
IOUT compliance voltage		Output current = 120mA	100			mV
Maximum output current	Imax		115	120	125	mA
Power on time				0.5		ms

Power on sequence

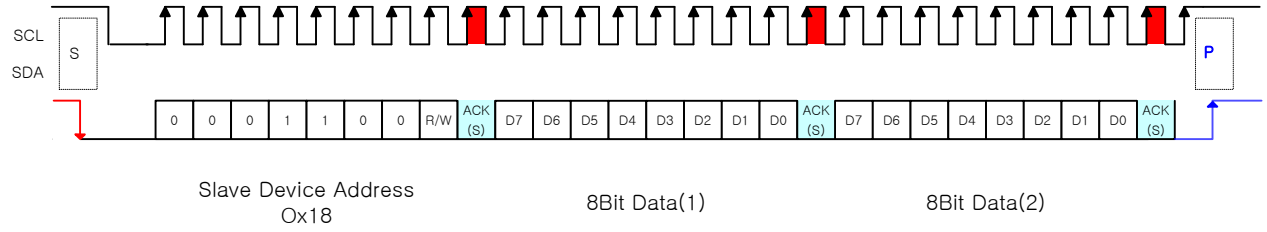


- XSD can be connect to VDD.

Resister

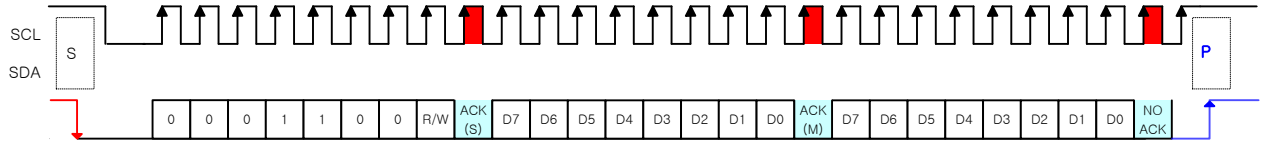
- I2C format

Write Operation



Slave Device Address Ox18 | 8Bit Data(1) | 8Bit Data(2)

Read Operation



Slave Device Address Ox19 | 8Bit Data(1) | 8Bit Data(2)

Within the procedure of the I2C-bus, unique situations arise which are defined as START (S) and STOP (P) conditions. A HIGH to LOW transition on the SDA line while SCL is HIGH is one such unique case. This situation indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition.

- Register Format

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data1	PD	FLAG	D9	D8	D7	D6	D5	D4
Data2	D3	D2	D1	D0	S3	S2	S1	S0

PD : Power down mode

PD	Codes per step
0	Normal operation mode
1	Power down mode

FLAG : FLAG must keep “L” at writing operation

D[9:0] : Input decoder data

Output current = (D[9:0]/1023) X 120mA

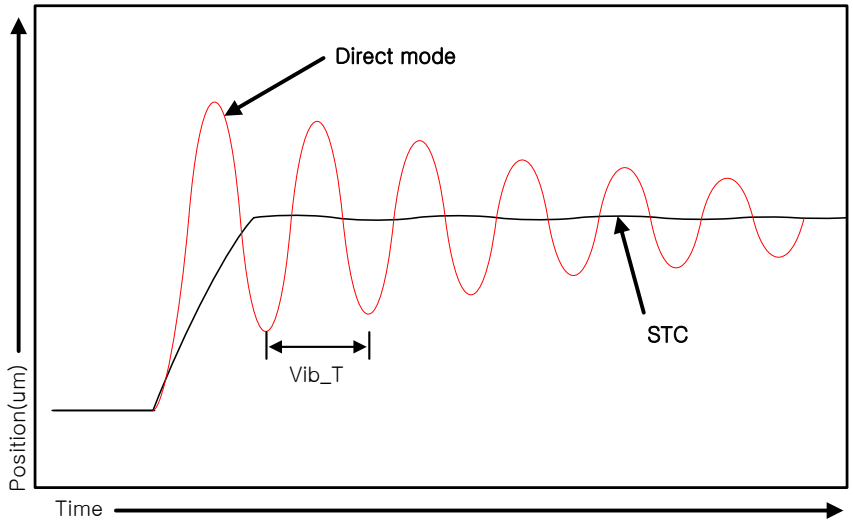
S[3:2] : Code per Step control

S[3:2]	Code per Step
00	Direct driving
01	1 step
10	2 step
11	4 step

S[1:0] : Smart transition control

S[1:0]	Transition time
00	Vib_T X 1
01	Vib_T X 2
10	Vib_T X 4
11	Vib_T X 8

Vib_T = Under the description



Vib_T Set up Method

- Vib_T Set on

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data1(OxEC)	1	1	1	0	1	1	0	0
Data2(OxA3)	1	0	1	0	0	0	1	1

- MCLK[1:0] setting

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data1(OxA1)	1	0	1	0	0	0	0	1
Data2(1)	0	0	0	0	0	1	MCLK[1]	MCLK[2]

(1) Default : 0x05

- T_Control[4:0] setting

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data1(OxF2)	1	1	1	1	0	0	1	0
Data2(2)	T_C[4]	T_C[3]	T_C[2]	T_C[1]	T_C[0]	0	0	0

(2) Defalut : 0x00

- Vib_T Set off

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data1(OxDC)	1	1	0	1	1	1	0	0
Data2(Ox51)	0	1	0	1	0	0	0	1

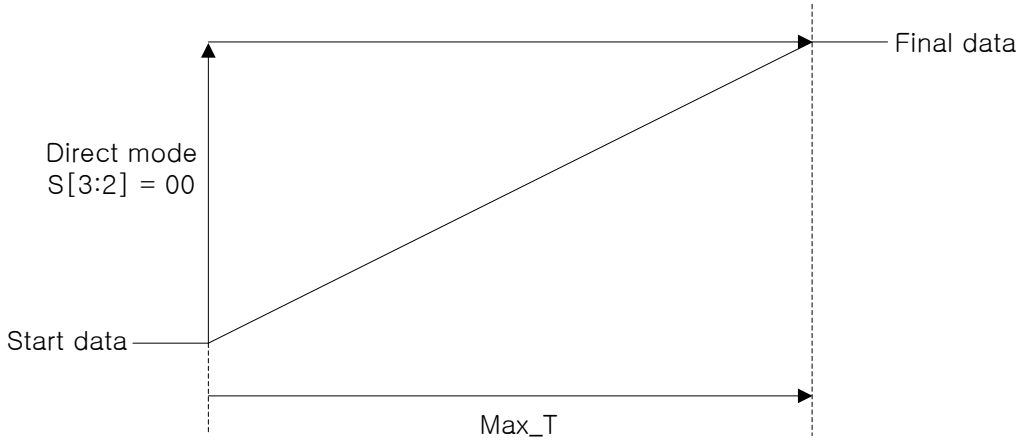
- Vib_T selection table

$$\text{Max\_T} = \frac{1023}{final\_data - start\_data} \text{ X Vib\_T}$$

T_Control[4:0] = 00000(default), MCLK(1)[1:0] = 01(default)

T_Control[4:0]	Max_T(ms)	T_Control[4:0]	Max_T(ms)
10000	139.0	00000 (default)	83.0
10001	133.0	00001	81.0
10010	128.0	00010	79.0
10011	123.0	00011	78.0
10100	119.0	00100	76.0
10101	115.0	00101	75.0
10110	111.0	00110	73.0
10111	106.0	00111	72.0
11000	103.0	01000	71.0
11001	100.0	01001	70.0
11010	98.0	01010	69.0
11011	94.0	01011	68.0
11100	91.0	01100	67.0
11101	89.0	01101	66.5
11110	87.0	01110	66.0
11111	85.0	01111	65.5

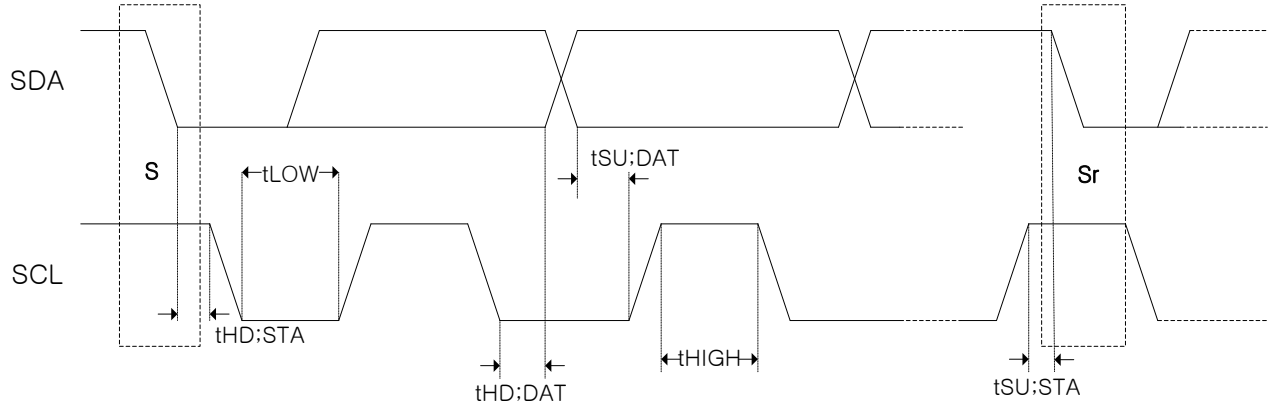
(1) MCLK[1:0] = 00 : double 01 : X1(default)
10 : half 11 : quarter

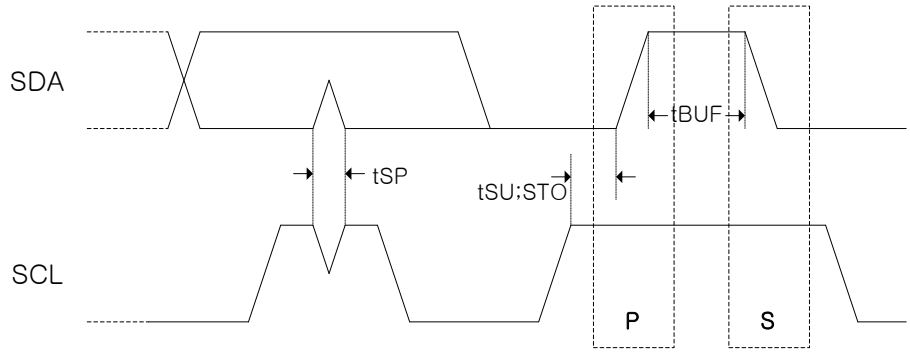


I2C Protocol

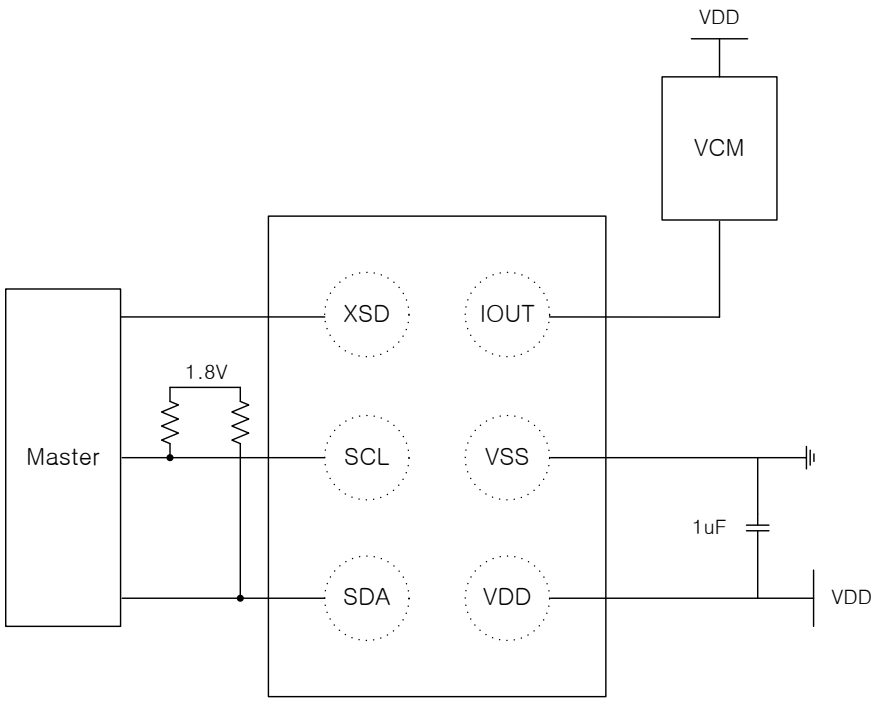
- I2C timing

Parameter	Symbol	Min	Max	Unit
SCL clock frequency	f_{SCL}	0	400	kHz
Hold time (repeated) START condition	$t_{HD;STA}$	0.6	–	us
Low period of the SCL clock	t_{LOW}	1.3	–	us
High period of the SCL clock	t_{HIGH}	0.6	–	us
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	–	us
Data hold time	$t_{HD;DAT}$	–	0.9	us
Data set-up time	$t_{SU;DAT}$	100	–	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	–	us
Bus free time between a STOP and START condition	t_{BUF}	1.3	–	us
Pulse width of spike suppress	t_{SP}	0	50	ns



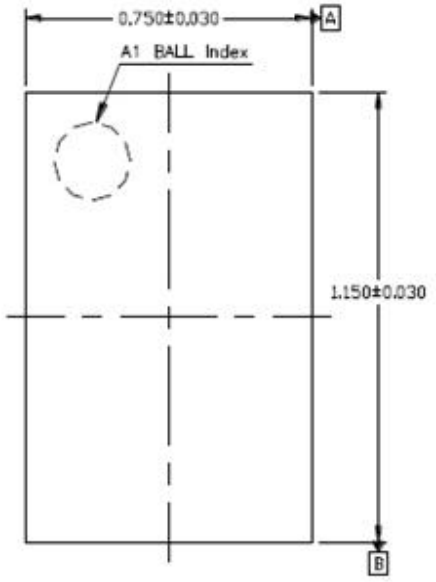


Application circuit

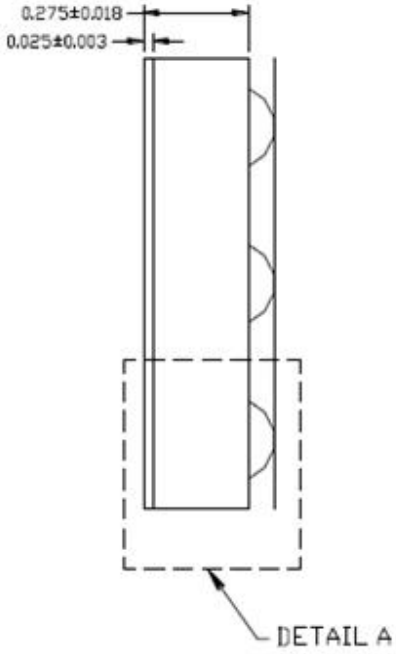


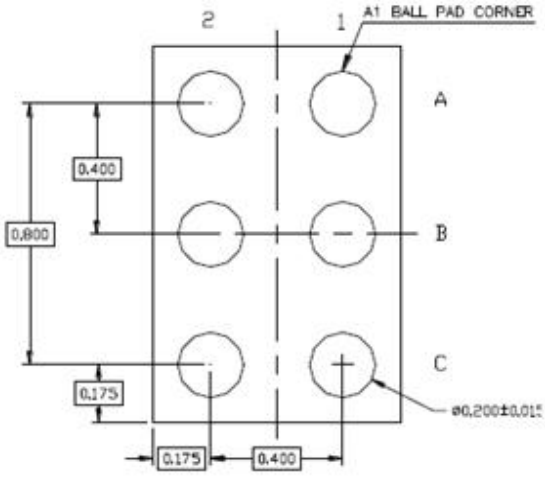
bottom View

Package Outline(6pin-WLP)

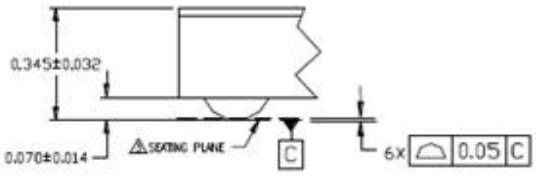


TOP VIEW





BOTTOM VIEW



DETAIL A
(ROTATED 90 DEG CW)