NXM5002

VCM Driver with Hall sensor

General Description

The NXM5002 is a one chip hall sensor driver.
It includes linear hall sensor, ADC, controller and actuator.
The NXM5002 has rotational movement detector in magnetic embedded system.
Because of that, It can operate with very high accuracy.
The Rotation movement detection method is a distinctive algorithm of NEXTLab.

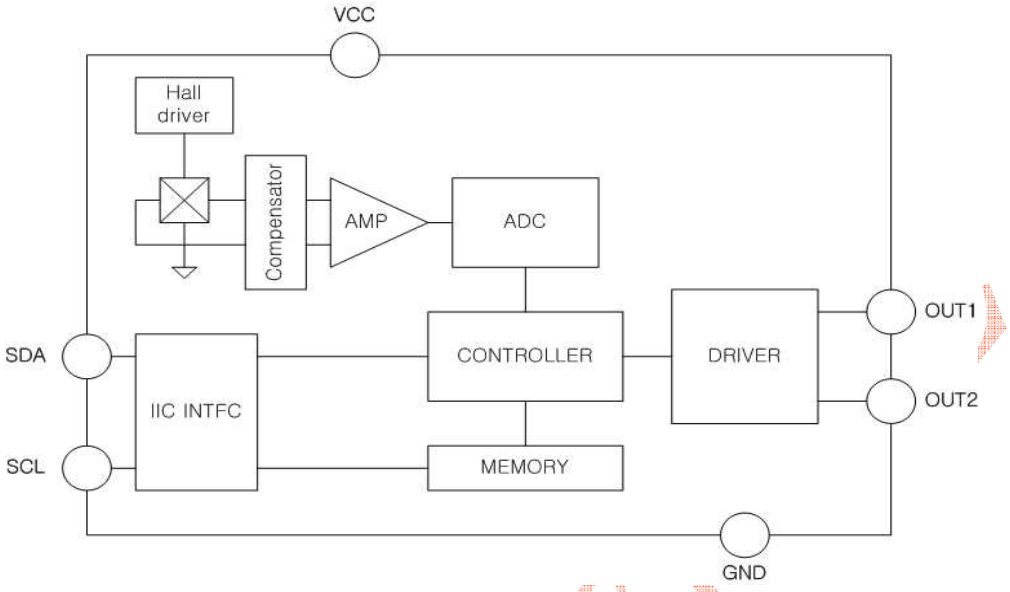
Feature

. Supply voltage : 2.4V ~ 3.6V
. IIC Interface : standard/fast mode
Default Slave address E0/E1 (W/R), Slave address can be set.
. **Embedded Hall sensor**
. **Self Auto-calibration with only one IIC command**
. **High speed non-volatile memory**
User free access : 96Byte
Speed of write only (max) : 2.0MHz (IIC bus speed)
Store (write complete) time (max) : 28mS
← One time Store automatically, after full (selected) byte write
Speed of read (max) : 2.0MHz (IIC bus speed)
Time of immediately Read after write (max) : 28mS
. PID controller
. **Position command bit : 10bit resolution**
. High accuracy position sensing.
. **Rotation movement error cancelation.**
. H bridged power out
. Power down mode
. **Hall sensor position output : 10bit**
. **FRA (Frequency Response Analysis) Function is supported**
. Package : 6-pin WL-CSP

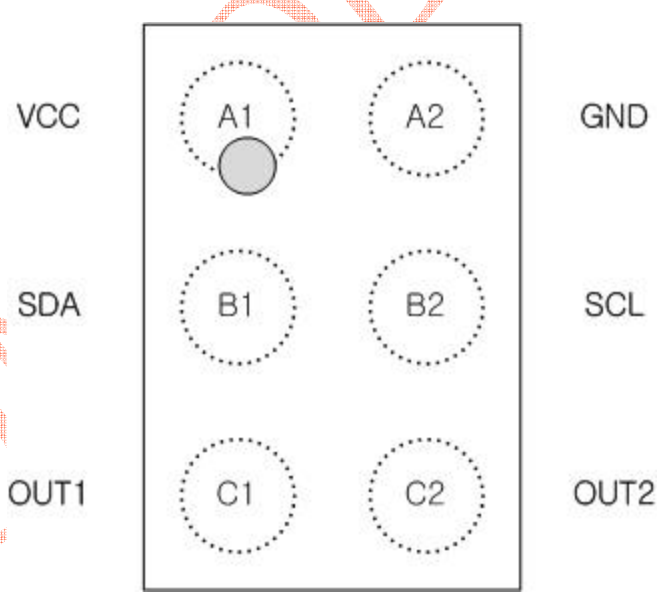
Application

. Mobile Magnetic application
. Camera phone

Block Diagram



Terminal assignment



Bumps down view

Pin description

Pin Name	Pin No.	I/O	Description
VCC	A1	S	Power Supply
GND	A2	S	Ground
SDA	B1	I/O	Serial Data for IIC
SCL	B2	I	Serial Clock Line for IIC
OUT1	C1	O	Actuator Driver out1
OUT2	C2	O	Actuator Driver out2

Maximum Absolute ratings

Parameter	Symbol	Value	Unit
Supply Voltage	Vddmax	-0.3 ~ 4.0	V
Maximum Pin voltage (Normal)	Vpnmax	-0.3 ~ Vdd+0.3	V
Maximum Pin voltage (Open Collector)	Vpomax	-0.3 ~ Vdd+0.3	V
Storage temperature	Tstg	-45 ~ 150	℃
Operating temperature	Topr	-40 ~ 85	℃
Power Dissipation	Pdmax	800	mW

ESD Characteristics

Mode	Polarity	Characteristic			unit
		min	typ	max	
HBM	Positive/Negative	2000	-	-	V
MM	Positive/Negative	200	-	-	V
CDM	Positive/Negative	800	-	-	V

Electrical Characteristics

VDD = 2.4~3.6V, Ta=-40~85℃ Unless otherwise noted

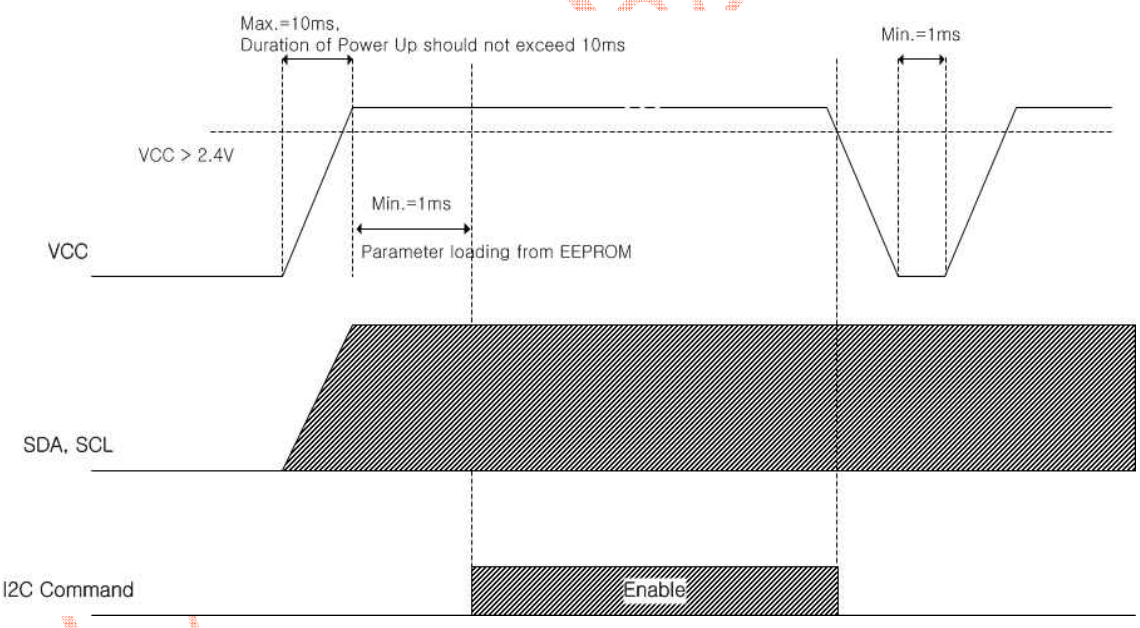
Characteristics	Symbol	Condition	Value			unit
			min	typ	max	
Operating supply voltage	Vcc	-	2.4	-	3.6	V
Self Auto calibration time	Tcal	-		400		ms
Current consumption	Icc1	Power down mode	-	2.5	6	uA
	Icc2	Normal mode, No load, Vcc=2.8V, Max ck	-	3.1	-	mA
	Icc3	High accuracy mode, No load, Vcc=2.8V	-	3.6	-	mA
	Icc4	Normal mode, No load, Vcc=3.3V, Max ck	-	3.5	-	mA
	Icc5	High accuracy mode, No load, Vcc=3.3V	-	3.9	-	mA

Electrical Characteristics (continued)

Characteristics	Symbol	Condition	Value			unit
			min	typ	max	
Start (Ready) time	Ts	After Enable	-	-	1.0	mS
Output load	Rl	-	15	-	-	Ω
Output current	Iout	Rl=22ohm	-	100	-	mA
Logic input low voltage	Vthl	-	0	-	0.4	V
Logic input high voltage	Vthh	-	1.2	-	Vcc	V
EEPROM						
Memory write speed	fw	Write only	-	-	2.0	MHz
Memory read speed	fr	Read only	-	-	2.0	MHz
Memory store complete time	Ts	-	-	-	28	mS
EEPRom Endurance	EEN1	Ta=25℃	100K			cycle
	EEN2	Ta=125℃	10K			cycle
EEPRom Data retention	ERE	-	10			year

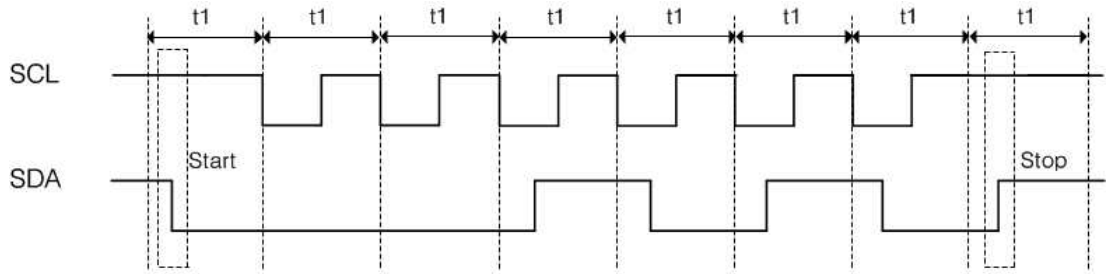
Sequence of Power Activation

The recommended sequence of power activation is below figure.



IIC Bus

- I2C Timing (SCL, SDA)



Timing :

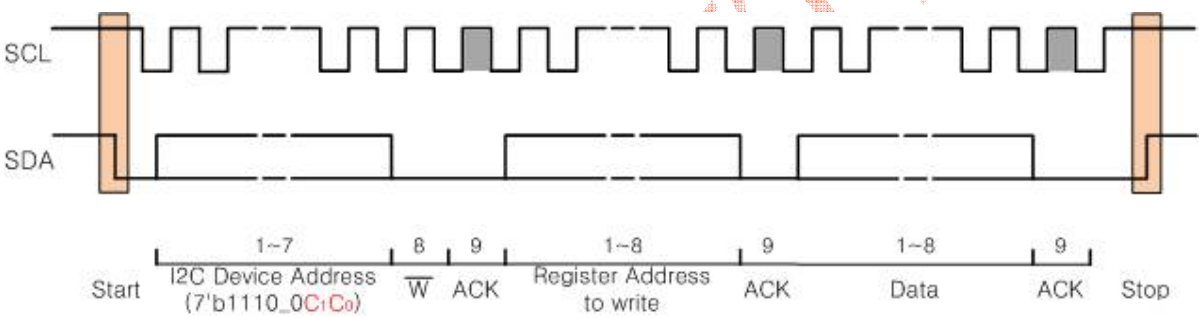
· TS = t1 = 0.5uS(2.0MHz) · NRZ = TS * 0.25

· R = TS * 0.5

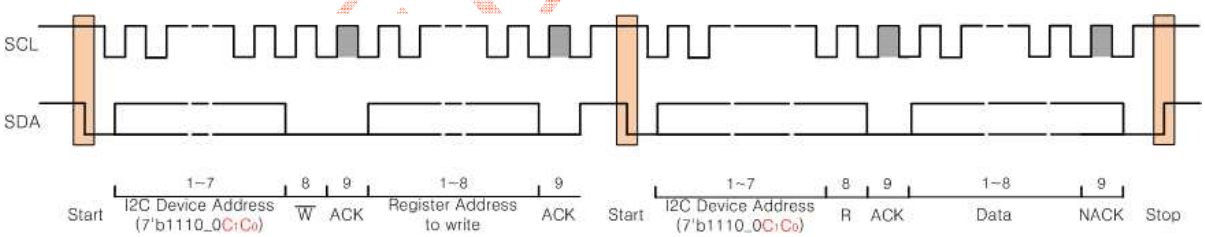
Duty :

· SCL = R · SDA = NRZ

- The timing flow of write mode is same below figure.



- **The timing flow of read mode is same below figure.**



Register Map

Address		R/W	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
Register	EPROM									
-	0x00~0x5F	R/W	Customer free access area (96byte)							
0x90	0x60		o_drvpol	o_selPos	o_hallsw	SysMD	o2_ackd		o2_dckd	
0x91	0x61		ResReg			o_gr				
0x92	0x62		Ev area				calLim[1:0]		o_selCo[1:0]	
0x93	0x63		NR			calD1				
0x94	0x64		calD2							
0x95	0x65		calD3							
0x96	0x66		NR			adjD1				
0x97	0x67					adjD2				
0x98	0x68		calD4L							
0x99	0x69		NR						calD4M	
0x9A	0x6A		calD5L							
0x9B	0x6B		NR						calD5M	
0x9C	0x6C								CB[1:0]	
0x9D	0x6D		Calconf		ADClpf		calC			
-	0x6E~0x7D		System Coefficient area							
-	0x7E~0x7F	-	EEProm cal area							
0x80		R/W	EVL			o_srst	oprMD[1:0]		o_drven	o_en
0x81			PosReg[7:0]							
0x82			calMD	NR		FRAen	NR		PosReg[9:8]	
0x83			EVL							
0x84		R	ADC[5:0]						NR	
0x85			NR		EEbusy	VMCS	ADC[9:6]			
0x86		R/W	Dinfra[7:0]							

: Device supplier evaluation, setting or device Self generating area

: Module manufacturer setting area with/without device supplier assistance

: Customer control area

: Customer free usable area

0x00 ~ 0x5F	R/W	Customer free access area (96byte)

- Customer useable area(96bytes)

0x90	0x60	R/W	o_drvpol	o_selPos	o_hallsw	SysMD	o2_ackd	o2_dckd

- o_drvpol : Driving polarity selection register

o_drvpol	Direction
1'b0	Postive
1'b1	Negative

- o_selPos : Position Data Format selection register

o_drvopt	Mode
1'b0	10.0 Format
1'b1	10.2 Format

- o_hallsw : Sub-Hall connection to Pre-amp selection register

o_hallswl	Connection
1'b0	Hall-P connects to positive input of Pre-amp Hall-N connects to negative input of Pre-amp
1'b1	Hall-N connects to positive input of Pre-amp Hall-P connects to negative input of Pre-amp

- SysMD : This register is useable for IC debugging

Customer should not access this register for normal operation

- o2_ackd : Analog to digital converter clock frequency selection register

o2_ackd[1]	o2_ackd[0]	Clock frequency
0	0	Divide by 1 (16MHz)
0	1	Divide by 2 (8MHz)
1	0	Divide by 4 (4MHz)
1	1	Divide by 8 (2MHz)

- o2_dckd : Digital clock frequency selection register

o2_ackd[1]	o2_ackd[0]	Clock frequency
0	0	Divide by 1 (16MHz)
0	1	Divide by 2 (8MHz)
1	0	Divide by 4 (4MHz)
1	1	Divide by 8 (2MHz)

0x91	0x61	R/W	ResReg	o_gr

- ResReg : Reserved Register
- o_gr : Gain of Pre-amp selection register

o_gr	Gain
0 ~ 31	X160 ~ X36 (4/step)

0x92	0x62	R/W	Ev area	calLim[1:0]	o_selCo[1:0]

- Ev area : This register is useable for IC debugging

Customer should not access this register for normal operation

- calLim : ADC noise cover range selection register on calibration

ADC output data is change minutely, in spite of equivalent input when calibration.

calLim[1]	calLim[0]	Range
0	0	±1LSB
0	1	±2LSB
1	0	±4LSB
1	1	±8LSB

- o_selCo[1:0] : Coefficients Changing range register

PID coefficients can be changed automatically to improve performance about overshoot and response when gap of ADC and posReg is less than set-up value.

o_selCo[1]	o_selCo[0]	Range
0	0	±4LSB
0	1	±8LSB
1	0	±12LSB
1	1	±16LSB

0x93	0x63	R/W	ResReg	calD1

- ResReg : Reserved Register
- calD1 : Pre-amp input offset calibration data

Value of calD1 is determined by module calibration operation or Manual write enable.

0x94	0x64	R/W	calD2

- calD2 : Module calibration data2

Input Current of hall is adjusted in value of calD2

Value of calD2 is determined by module calibration operation or Manual write enable.

0x95	0x65	R/W	calD3

- calD3 : Module calibration data3

Reference voltage of ADC is adjusted in value of calD3

Value of calD3 is determined by module calibration operation or Manual write enable.

0x96	0x66	R/W	ResReg	adjD1

- ResReg : Reserved Register
- adjD1 : Band-Gap Voltage adjustment register (Manufacturer adjustment)

0x97	0x67	R/W	ResReg	adjD2

- ResReg : Reserved Register
- adjD2 : OSC frequency adjustment register (Manufacturer adjustment)

0x98	0x68	R/W	calD4L	
0x99	0x69		ResReg	calD4M

- calD4 : 10-bit ADC remain offset data after Pre-amp offset calibration

This register is used for rotation error correction.

0x9A	0x6A	R/W	calD5L	
0x9B	0x6B		ResReg	calD5M

- calD5 : 10-bit ADC data of sub-hall after Full calibration operation is ended

This register is used for rotation error correction.

0x9C	0x6C	R/W	ResReg	CB[1:0]

- ResReg : Reserved Register
- CB : I2C custom bit register

CB[1]	CB[0]	Slave Address(W/R)
0	0	0xE0 / 0xE1
0	1	0xE2 / 0xE3
1	0	0xE4 / 0xE5
1	1	0xE6 / 0xE7

0x9D	0x6D	R/W	Calconf	ADClpf	calC

- Calconf : Calibration configuration, Use manufacturer recommended value.(2'b11)

- ADClpf : ADC filter configure register

ADClpf[1]	ADClpf[0]	Cutoff Frequency
0	0	0.6KHz @16MHz
0	1	1.2KHz @16MHz
1	0	2.4KHz @16MHz
1	1	Bypass

- calC : Calibration error flag register

  calC[3] : Pre-amp offset calibration error register

  calC[2] : Hall offset calibration error register 1 *

  calC[1] : Hall gain calibration error register

  calC[0] : Hall offset calibration error register 2 *

  If calibration operation is operated abnormally, this bits are will be set.

  * Hall offset operation is implemented twice for enhancing accuracy

-	0x6E~ 0x7D	R/W	System Coefficient area

- System Coefficient area : This registers are used for PID controller

-	0x7E~ 0x7F	-	EEProm cal area

- EEProm cal area : This registers are used for EEProm

  Customer should not access to this register

0x80	-	R/W	EVL	o_srst	oprMD[1:0]	o_drven	o_en

- EVL : This register is useable for IC debugging

  Customer should not access to this register for normal operation

- o_srst : Software Reset

  When this register is high status, all blocks reset and then it will be clear automatically

- oprMD : Operation accuracy selection register

  This register is used to select VMCS range, (Actuator movement OK signal.)

oprMD[1]	oprMD[0]	Range
0	0	±1LSB
0	1	±2LSB
1	0	±3LSB
1	1	±4LSB

- o_drven : Output Driver Enable register

  When this register is set, output driver is enabled

- o_en : Analog block Enable register(Reference block, OSC, ADC, etc..)

  When this register is set, analog block is enabled

0x81	-	R/W	PosReg[7:0]					
0x82	-		calMD	NR		FRAen	NR	PosReg[9:8]

- PosReg : 10-bit target position register

- calMD : Calibration operation start register
  When this register is set, calibration is implemented
  This register is clear automatically after calibration completion

- FRAen : Frequency Response Analysis enable.
  If this register is set,
  Main feedback will be off, and the H bridge output is controlled by Dinfra value

0x83	-	R/W	EVL

- EVL : This register is useable for IC debugging

0x84	-	R	ADC[5:0]				NR
0x85	-		NR	EEbusy	VMCS	ADC[9:6]	

- ADC : ADC output register
- NR : Not reserved
- EEbusy : EEProm Busy register
  When this register is low status, you shouldn't access into EEProm
- VMCS : Actuator movement completion register
  This registers are read only
  even if this register is high, the PID feedback operation is ongoing.

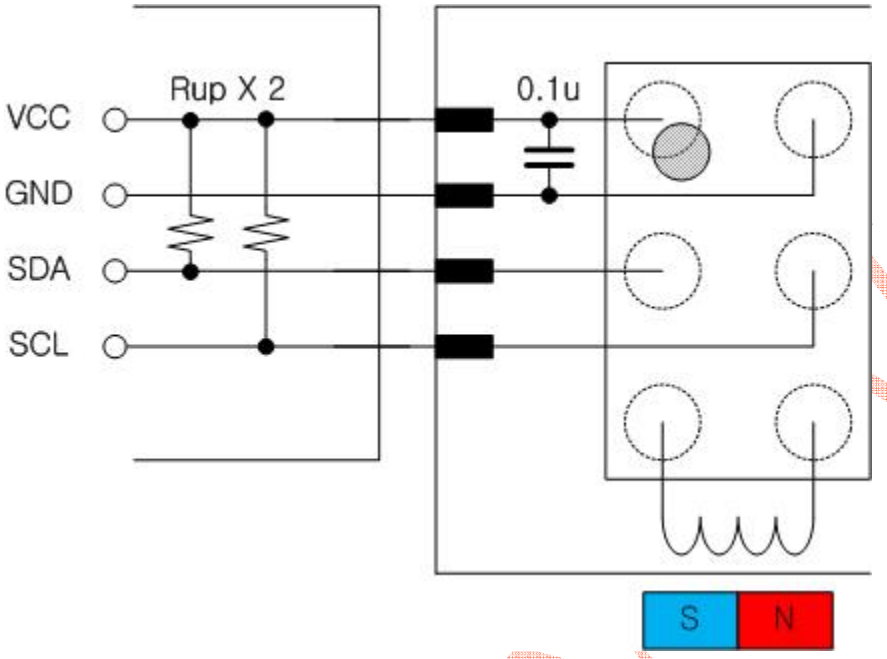
0x86		R/W	Dinfra[7:0]

- Dinfra : Output data register when FRAen is set.
  The output voltage is determined by this register value.

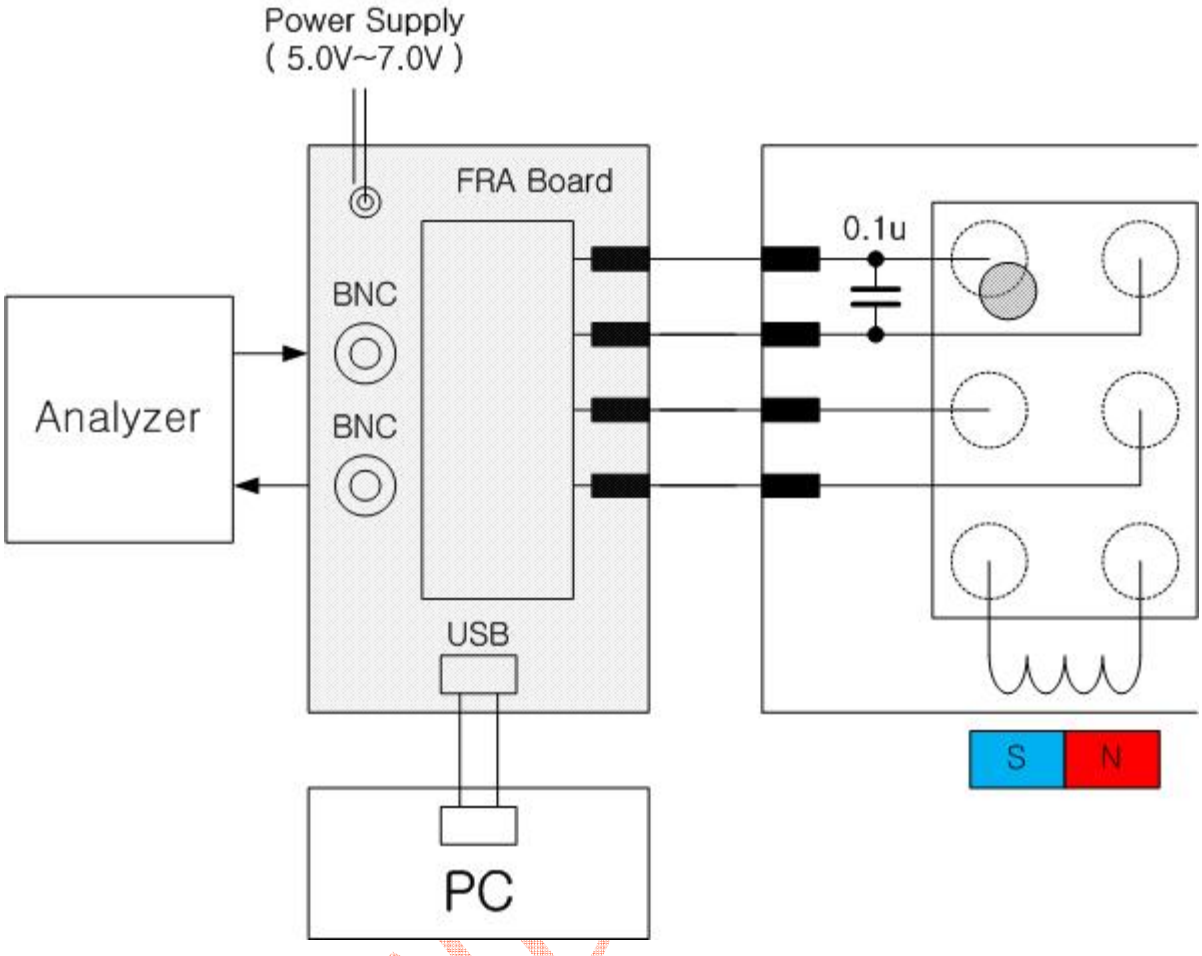
Frequency Response Analysis

This option is for measuring module`s frequency response.
If FRAen(0x82[4]) is set, this option should be enable.
You can control driving power to change Dinfra(0x86) value.
According to changing of input frequency(Dinfra),
you can monitor continuously changed ADC value(0x84&0x85) that represents module`s position.
You can estimate module`s frequency response, as you analyze ADC value.

Application Circuit



FRA (Frequency Response Analysis) Circuit



Package Outline (6-WL-CSP)

Package Outline					
Package Thickness (a)	275±32 um	Bump Pitch			400 um
Wafer Thickness (a1)	200±15 um	Package Size (D x E)			D=730±15 um, E=1,130±15 um
Ball Height (a2)	50±14 um	Ball Diameter (s)			200±24 um
Back Side Coating Thickness	25±3 um	Kerf Width			50 um
Distance from Bump Center to Package Edge		f 1	165 um	f 3	165 um
		f 2	165 um	f 4	165 um
Customer POD Drawing No./ Rev. No.		N/A			
Description