1. INTRODUCTION

1.1 Introduction

NXM2011 is a best audio-processing power amplifier solution for mobile application which has both digital audio interface and analog audio interface. It has 1.5W/ch. Filter-less stereo loud-speaker digital amplifier for stereo 8Ω speakers, stereo headphone amplifier for up to 16Ω headphone, mono ear speaker(receiver) amplifier for receiver 32Ω speaker, and stereo line out signal for external amplifier and etc.. NXM2011 supports 2-port digital input (I2S/PCM) and 2-port stereo analog input signals. Asynchronous sample rate converter (ASRC) and enhanced stereo 3D functions are integrated on-chip. This device changes I2S compatible PCM data into PWM signal (CPP™). NXM2011 supports I2C/SPI serial control interface to communicate with MCU.

NXM2011 has the internal processing capability for 3-channel digital signal (main stereo channel and mono voice channel). The 2-port digital input signals are re-sampled by ASRC and this re-sampled signals can be mixed by 3x4 gain matrix (input mixer) to make internal 3-channel signals (internal left/right/voice channel). Re-sampled left/right data (fs=48kHz) of port1 can be serial-out to port0 with I2S interface. It supports stereo enhancement 3D-effect, 7-band equalizer, tone control (bass/treble), deemphasis, loudness compensation, soft volume and AGC (automatic gain control). Download of filter coefficients is available through I2C/SPI interface for EQ/Bass/Treble filter, therefore parametric EQ can be implemented. It has also output mixer to mix digital signals and analog signals. Therefore the processed internal signals can be mapped to various output amplifiers.

1.2 Applications

- 2.5G and 3G Mobile Phones and Multimedia terminals
- PDA, Internet Appliances and Portable Gaming
- Portable DVD/CD/AAC/MP3 Players
- Digital Cameras and Toys

1.3 Features

1.3.1 Output Power @ 5.5V, THD+N=1%

- Loud Speaker : 1.5W x 2CH @ 8Ω
- Headphone : 80mW x 2CH @ 16Ω
- Ear Speaker : 350mW x 1CH @ 32Ω
- Stereo analog output for line out
- Filter-less speaker connection
- DC Cap-less headphone connection

1.3.2 Digital Input

- 2-Port Digital Audio inputs (I2S/PCM)
- Supported I2S compatible formats
- Supported PCM data formats (long/short frame)
- 8,12,13,16,18,20,24 bit supported
- Sample rates supported 8kHz~48kHz

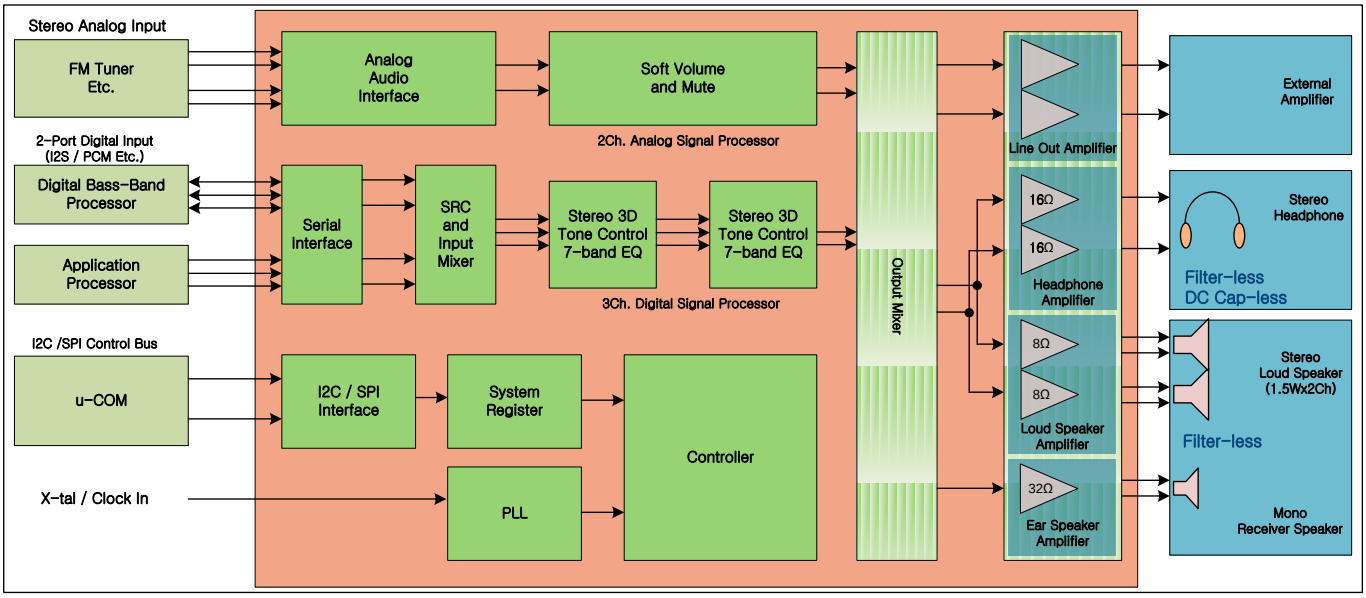
1.3.3 Analog Input

- 2-Port Stereo Analog Inputs

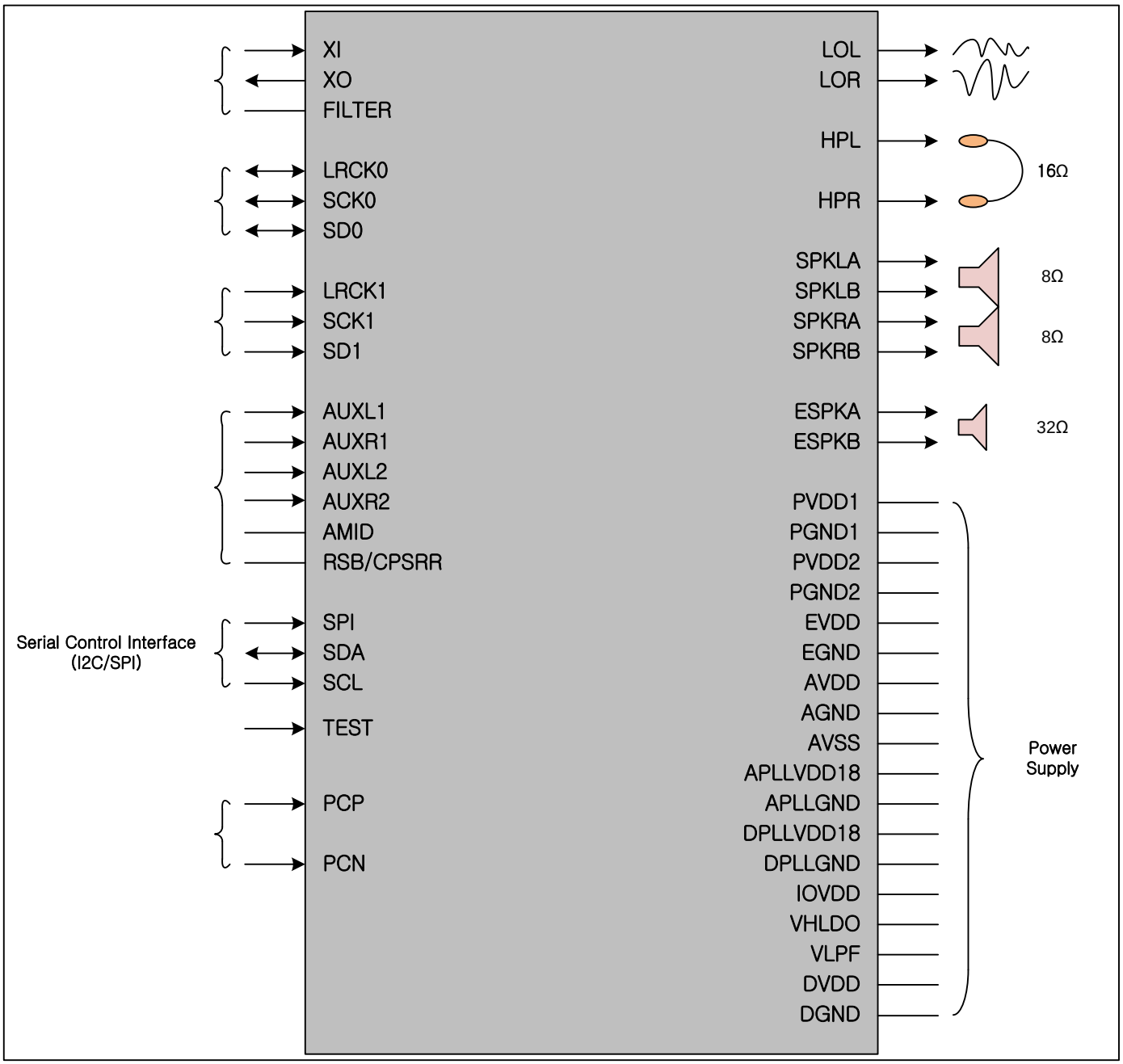
1.3.4 Functions

- Sample rate converter imbedded : Fs=8kHz~48kHz
- Full 3x4 input gain matrix for input mixer
- Stereo enhancement 3D-Effect for headphone/speaker
- 7-band Equalizer : +12dB~-12dB, 2dB step
- Tone control (Bass/Treble) : +12dB~-12dB, 2dB step
- EQ/Bass/Treble filter coefficients download available.
- Deemphasis filter
- Loudness Compensation
- Soft volume / soft-mute : +24db~-70dB and -∞, 0.5dB step
- Automatic Gain Control (AGC) for non-clipping
- Output mixer and adjustable amplifier gain.
- Ground-referenced Output to eliminate DC-Bias on Headphone Amplifier
- DC-blocking capacitor-less direct headphone driver with Charge-pump & LDO.
- Power down mode supported.
- Package : 4x4mm^2 49-pin BGA

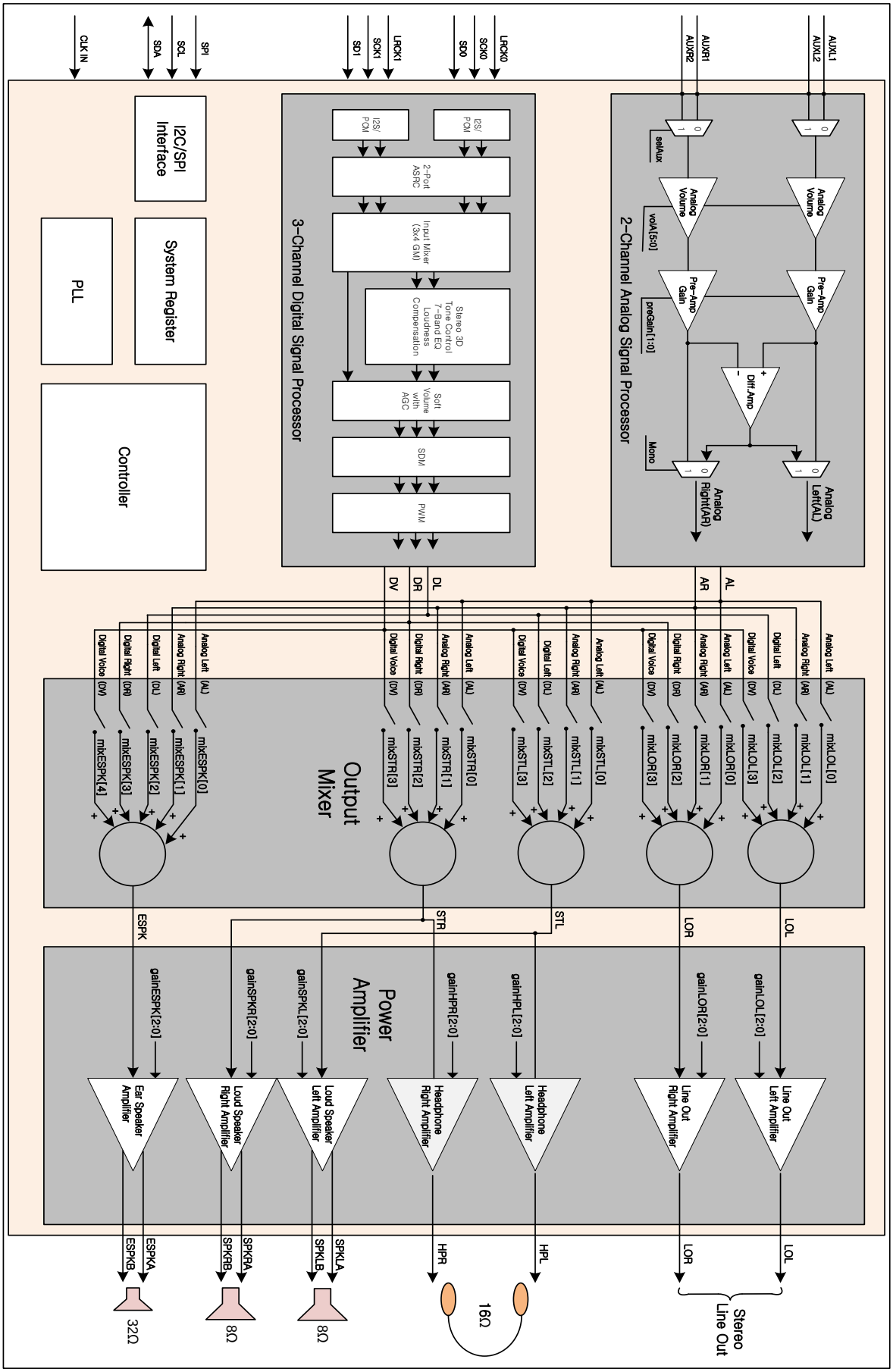
1.4 Block Diagram



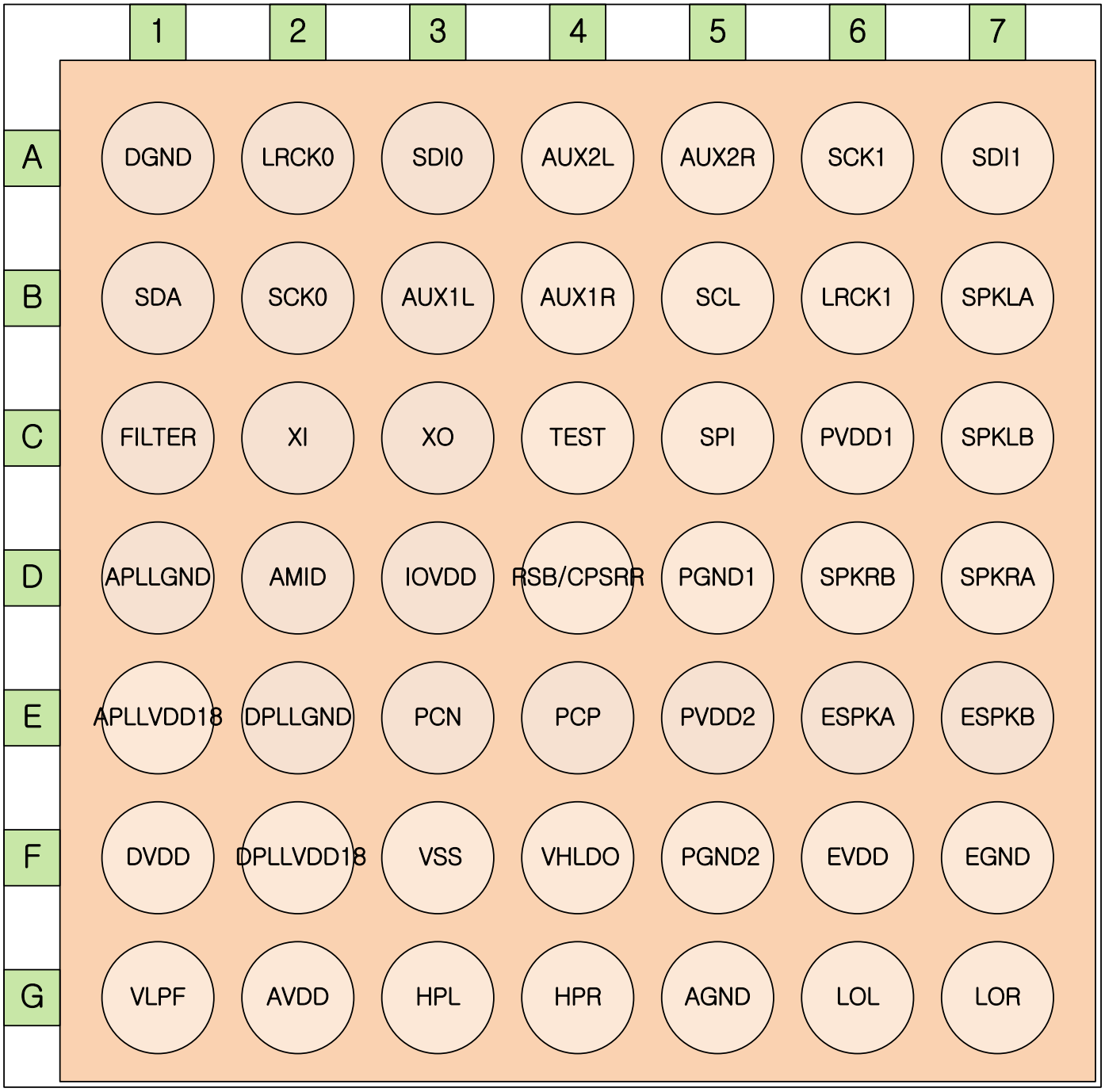
1.5 Signal Interface Diagram



1.6 Detailed Internal Block Diagram



1.7 Pin Assignment



1.8 Pin Description

Name	Number	Type	Description	
Power and Ground				
AVDD	**G2**	**P**	3.0~5.5V Power for Analog processing block	
AGND	**G5**	**G**	3.0~5.5V Ground for Analog processing block	
IOVDD	**D3**	**P**	Selectable Power for IO	
DVDD	**F1**	**P**	1.8V Digital Power for core logic	
VLPF	**G1**	**P**	1.8V Power for Analog processing block	
DGND	**A1**	**G**	Digital Ground for IO and core logic	
PVDD1	**C6**	**P**	3.0~5.5V Power1 for Power Amplifier block	
PVDD2	**E5**	**P**	3.0~5.5V Power2 for Power Amplifier block	
PGND1	**D5**	**G**	3.0~5.5V Ground1 for Power Amplifier block	
PGND2	**F5**	**G**	3.0~5.5V Ground2 for Power Amplifier block	
EVDD	**F6**	**P**	3.0~5.5V Power for ESPK Amplifier block	
EGND	**F7**	**G**	3.0~5.5V Ground for ESPK Amplifier block	
APLLVDD18	**E1**	**P**	1.8V Power for Analog block of PLL	
DPLLVDD18	**F2**	**P**	1.8V Power for Digital block of PLL	
APLLGND	**D1**	**G**	1.8V Ground for Analog block of PLL	
DPLLGND	**E2**	**G**	1.8V Groud for Digital block of PLL	
Clock and PLL				
XI	**C2**	**I**	Clock Input / X-tal Input	
XO	**C3**	**O**	X-tal Output	
FILTER	**C1**	**IO**	External loop filter network input for PLL	
Serial Control Interface				
SPI	**C5**	**I**	I2C/SPI selection pin If high, I2C mode and if low, SPI mode (low-active chip select pin at SPI mode). High-to-low transition means SPI start and low-to-high transition means SPI end.	
SCL	**B5**	**I**	Serial clock at both I2C and SPI. SDA data bit valid at rising edge of SCL at SPI mode.	
SDA	**B1**	**IO**	Serial data bit at both I2C and SPI mode.	
Analog Processing IO				
VHLDO	**F4**	**O**	1.6 ~ 2.5V LDO Output for Headphone Amplifier	
VSS	**F3**	**O**	-1.6 ~ -2.5V Negative Output for Headphone Amplifier	
PCP	**E4**	**IO**	Positive Flying capacitor network input for Charge-pump block	
PCN	**E3**	**IO**	Negative Flying capacitor network input for Charge-pump block	
VLPF	**G1**	**O**	1.8V LDO Output for LPF block	
Test				
TEST	**C4**	**I**	This pin is for Test and must be low for normal operation.	
Digital Audio Serial Interface				
LRCK0	**A2**	**IO**	Left/Right word clock for port0. Fs=8kHz~48kHz available.	
SCK0	**B2**	**IO**	Serial bit clock for port0.	
SD0	**A3**	**IO**	Serial data bit for port0.	
LRCK1	**B6**	**I**	Left/Right word clock for port1. Fs=8kHz~48kHz available.	
SCK1	**A6**	**I**	Serial bit clock for port1.	

SD1	**A7**	**I**	Serial data bit for port1.	
Analog Audio Interface				
AUXL1	**B3**	**I**	Left channel analog audio single-ended input1. Differential input available by using AUXL1 and AUXR1. (AUXL1 : positive, AUXR1 : negative). Single-Ended mode / Differential mode selectable.	
AUXL2	**A4**	**I**	Left channel analog audio single-ended input2. Differential input available by using AUXL2 and AUXR2. (AUXL2 : positive, AUXR2 : negative). Single-Ended mode / Differential mode selectable.	
AUXR1	**B4**	**I**	Right channel analog audio single-ended input1. Differential input available by using AUXL1 and AUXR1. (AUXL1 : positive, AUXR1 : negative). Single-Ended mode / Differential mode selectable.	
AUXR2	**A5**	**I**	Right channel analog audio single-ended input2. Differential input available by using AUXL2 and AUXR2. (AUXL2 : positive, AUXR2 : negative). Single-Ended mode / Differential mode selectable.	
AMID	**D2**	**I**	Analog middle (center) voltage for virtual ground.	
RSB/CPSRR	**D4**	**I**	External Reset (low-active reset) and Analog clean voltage for the best PSRR.	
Amplifier Output				
LOL	**G6**	**O**	Line Out Left channel Amplifier.	
LOR	**G7**	**O**	Line Out Right channel Amplifier.	
SPKLA	**B7**	**O**	Loud Speaker Left channel Amplifier A. Up to 8Ω speaker available. Left channel Loud speaker connected between SPKLA and SPKLB.	
SPKLB	**C7**	**O**	Loud Speaker Left channel Amplifier B. Up to 8Ω speaker available. Left channel Loud speaker connected between SPKLA and SPKLB.	
SPKRA	**D7**	**O**	Loud Speaker Right channel Amplifier A. Up to 8Ω speaker available. Left channel Loud speaker connected between SPKLA and SPKLB.	
SPKRB	**D6**	**O**	Loud Speaker Right channel Amplifier B. Up to 8Ω speaker available. Left channel Loud speaker connected between SPKLA and SPKLB.	
HPL	**G3**	**O**	Headphone Left channel Amplifier. If headphone is connected between HPL/HPR and VCOM, DC-blocking capacitor is not needed.	
HPR	**G4**	**O**	Headphone Right channel Amplifier. If headphone is connected between HPL/HPR and VCOM, DC-blocking capacitor is not needed.	
ESPKA	**E6**	**O**	Ear speaker (for voice) mono Amplifier A. up to 32Ω speaker available. Ear speaker connected between ESPKA and ESPKB.	
ESPKB	**E7**	**O**	Ear speaker (for voice) mono Amplifier B. up to 32Ω speaker available. Ear speaker connected between ESPKA and ESPKB.	

Note. IO Description

I:Input O:Output IO:Bidirection (Input/Output) P:Power G:Ground

1.9 Electrical Characteristics

1.9.1 Absolute Maximum Ratings

Symbol	Description	Min	Max	Units
AVDD	Power supply for analog block	-0.5	6.5	V
IOVDD	Power supply for digital IO power	-0.5	6.5	V
DVDD	Power supply for digital core logic power	-0.5	2.3	V
PVDD1/PVDD2/EVDD	Power supply for power amplifier block and ear speaker amplifier block	-0.5	6.5	V
APLLVDD18	Power supply for PLL analog power	-0.5	2.3	V
DPLLVDD18	Power supply for PLL digital power	-0.5	2.3	V
T_{stg}	Storage Temperature	-65	+150	℃

1.9.2 Recommended Operating Conditions

Symbol	Description	Min	Typ	Max	Units
AVDD	Power supply for analog block	3.0	3.6	5.5	V
IOVDD	Power supply for digital IO power	3.0	3.6	5.5	V
DVDD	Power supply for digital core logic power	1.62	1.8	1.98	V
PVDD1/PVDD2/EVDD	Power supply for amplifier block	3.0	3.6	5.5	V
APLLVDD18	Power supply for PLL analog power	1.62	1.8	1.98	V
DPLLVDD18	Power supply for PLL digital power	1.62	1.8	1.98	V
T_{opr}	Storage Temperature	-40	+25	+85	℃

1.9.3 Electrical Characteristics

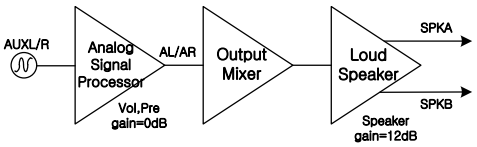
Parameter	Min	Typ	Max	Units
Input leackage current except for pull-up, pull-down input	-	-	300	uA
Input low voltage except for Schmitt input	-	-	0.30*IOVDD	V
Input high voltage except for Schmitt input	0.70*IOVDD	-	-	V
Input low voltage for Schmitt input (IOVDD = 3.6V)	1.14	1.26	1.38	V
Input high voltage for Schmitt input (IOVDD = 3.6V)	2.06	2.28	2.40	V
Output low voltage (IOVDD = 3.6V)	-	-	0.4	V
Output high voltage (IOVDD = 3.6V)	2.8	-	-	V
Input capacitance		1.6	4	pF
Output capacitance		1.6	4	pF
Input resistance of analog audio input, AUXL1, AUXL2, AUXR1 and AUXR2		40		kΩ

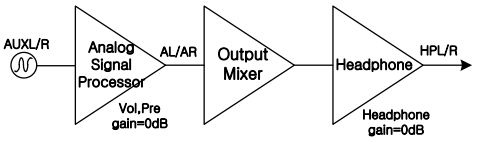
1.9.4 Operating Characteristics

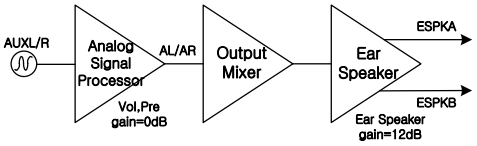
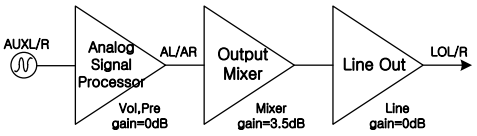
Test conditions

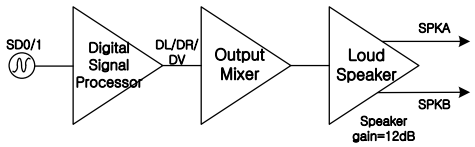
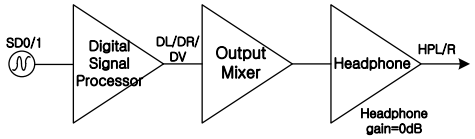
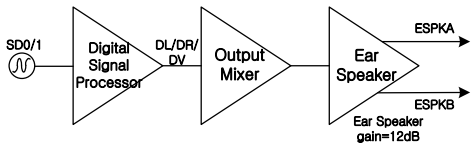
DVDD=APLLVDD18=DPLLVDD18=1.8V, IOVDD=3.3V, AVDD=PVDD1=PVDD2=EVDD=3.6V, VHLDO=2.5V, 1kHz Signal, fs=48kHz, AES17 Filter A-weight filter

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Analog Input							
Analog Input Path to Speak driver (8Ω Load)							
Output offset voltage	Vos	Inputs terminated to GND			±12		mV
Po (Output Power, THD+N=1%)	Po (THD=1%)	PVDD=5.5V			1.5		W
		PVDD=4.2V			0.85		
		PVDD=3.6V			0.63		
Total harmonic distortion +Noise	THD+N	Po=250mW, f=1kHz			0.04		%
		Po=250mW, f=20Hz			0.01		
Cross Talk	CT	Po=250mW, F=1kHz			-		dB
Noise output voltage	Vn	Inputs terminated to GND			60		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-70		dB
Analog Input Path to Headphone driver (16Ω Load)							
Output offset voltage	Vos	Inputs terminated to GND			±8		mV
Po (Output Power, THD+N=1%)	Po (THD=1%)	PVDD=5.5V			80		mW
		PVDD=4.2V			-		
		PVDD=3.6V			-		
Total harmonic distortion +Noise	THD+N	Po=20mW, f=1kHz			0.05		%
		Po=20mW, f=20Hz			0.03		
Cross Talk	CT	Po=20mW, F=1kHz			-75		dB
Noise output voltage	Vn	Inputs terminated to GND			19		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-85		dB

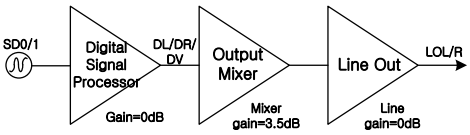




Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Analog Input Path to Ear Speak driver (32Ω Load)							
Output offset voltage	Vos	Inputs terminated to GND			±12		mV
Po (Output Power, THD+N=1%)	Po	PVDD=5.5V			0.35		W
		PVDD=4.2V			0.21		
		PVDD=3.6V			0.16		
Total harmonic distortion +Noise	THD+N	Po=60mW, f=1kHz			0.04		%
		Po=60mW, f=20Hz			0.01		
Noise output voltage	Vn	Inputs terminated to GND			60		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-70		dB
Analog Input Path to Line Out (10kΩ Load)							
Output offset voltage	Vos	Inputs terminated to GND			-		mV
Total harmonic distortion +Noise	THD+N	Vo=1Vrms, f=1kHz			0.007		%
		Vo=1vrms, f=20Hz			0.004		
Cross Talk	CT	Vo=1Vrms f=1kHz			-70		dB
Noise output voltage	Vn	Inputs terminated to GND			18		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-70		dB
Digital Input							
Digital Input Path to Speak driver (8Ω Load)							
Output offset voltage	Vos	Inputs terminated to GND			±20		mV
Po (Output Power, THD+N=1%)	Po	PVDD=5.5V			1.5		W
		PVDD=4.2V			0.85		
		PVDD=3.6V			0.63		

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Total harmonic distortion +Noise	THD+N	Po=250mW, f=1kHz			0.07		%
		Po=250mW, f=20Hz			0.05		
Cross Talk	CT	Po=250mW, F=1kHz			-		dB
Noise output voltage	Vn	Inputs terminated to GND			85		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-70		dB
Digital Input Path to Headphone driver (16Ω Load)							
Output offset voltage	Vos	Inputs terminated to GND			±14		mV
Po (Output Power, THD+N=1%)	Po	PVDD=5.5V			80		mW
		PVDD=4.2V			-		
		PVDD=3.6V			-		
Total harmonic distortion +Noise	THD+N	Po=20mW, f=1kHz			0.09		%
		Po=20mW, f=20Hz			0.07		
Cross Talk	CT	Po=20mW, F=1kHz			-75		dB
Noise output voltage	Vn	Inputs terminated to GND			29		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-85		dB
Digital Input Path to Ear Speak driver (32Ω Load)							
Output offset voltage	Vos	Inputs terminated to GND			±20		mV
Po (Output Power, THD+N=1%)	Po	PVDD=5.5V			0.35		W
		PVDD=4.2V			0.21		
		PVDD=3.6V			0.16		
Total harmonic distortion +Noise	THD+N	Po=60mW, f=1kHz			0.07		%
		Po=60mW, f=20Hz			0.05		

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Noise output voltage	Vn	Inputs terminated to GND			85		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-70		dB
Digital Input Path to Line Out (10kΩ Load)							
Output offset voltage	Vos	Inputs terminated to GND			-		mV
Total harmonic distortion +Noise	THD+N	Vo=1Vrms, f=1kHz			0.05		%
		Vo=1Vrms, f=20Hz			0.03		
Cross Talk	CT	Vo=1Vrms			-70		dB
Noise output voltage	Vn	Inputs terminated to GND			24		uVrms
Power Supply Rejection Ratio	PSRR	PVDD =0.1Vp-p, 217Hz			-70		dB
Analog Reference							
Mid Voltage	AMid			1/2AVDD			V
Start-up time		Analog Path Shut down			100us		us
Thermal shutdown		Threshold			150		℃
		Hysteresis			30		℃
Charge pump & LDO for Headphone Driver							
Charge pump switching frequency	fosc	freqOSC=0			500		kHz
		freqOSC=0			700		kHz
LDO Output Voltage	VHLDO	VHLDO[1:0]: 00			2.5		V
		VHLDO[1:0]: 10			1.9		V



1.9.5 Current Consumption

Test conditions

DVDD=APLLVDD18=DPLLVDD18=1.8V, IOVDD=3.3V, AVDD=PVDD1=PVDD2=EVDD=3.6V, VHLDO=2.5V, No Signal, fs=48kHz

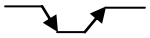
MODE	AVDD	PVDD1	PVDD2	EVDD	Unit
Reset mode	0	0	0	0	uA

Normal operation mode(Test pin=High) and Digital Reset	0.23	-	-	-	mA
Digital Processor On	10.7	-	-	-	
Digital Processor on & Analog Audio Source Block enable	12.1	-	-	-	
Digital Processor on & Analog Audio Source Block enable & LO Driver enable	14.7	-	-	-	
Digital Processor on & Analog Audio Source Block enable & Ear Speaker Driver enable	14.0	-	-	0.8	
Digital Processor on & Analog Audio Source Block enable & Loud Speaker Driver enable	14.0	1.0	1.0	-	
Digital Processor on & Analog Audio Source Block enable & Headphone Driver enable	21.9	-	-	-	
Digital Processor on & Analog Audio Source Block enable & All Driver enable	29.3	1.0	1.0	0.8	
Digital Processor On & LRV LPF enable	15.4	-	-	-	
Digital Processor On & LRV LPF enable & LO Driver enable	17.9	-	-	-	
Digital Processor On & LRV LPF enable & Ear Speaker Driver enable	17.3	-	-	0.8	
Digital Processor On & LRV LPF enable & Loud Speaker Driver enable	17.3	1.0	1.0	-	
Digital Processor On & LRV LPF enable & Headphone Driver enable	25.2	-	-	-	
Digital Processor On & LRV LPF enable & All Driver enable	32.6	1.0	1.0	0.8	
All Block Enable	33.9	1.0	1.0	0.8	

2. MCU INTERFACE

2.1. General Description

MCU interface is needed to determine the operation mode of this chip. It basically supports I2C Interface. Additionally SPI control interface is supported also, considering that I2C interface is not available. I2C interface supports read and write mode but SPI control interface supports only write mode. Interface type is determined by SPI pin as follows.

SPI	Interface Type
1 (always high)	I2C interface
 (low-active chip select signal)	SPI interface

2.1.1 Device Address at I2C interface

Device address is used to select this chip on I2C bus. This address consists of 8-bit length. LSB 1-bit determines read or write mode. If the LSB 1-bit is low, write mode is selected.

Device Address	Interface Type
1101_1100(0xDC)	Write mode
1101_1101(0xDD)	Read mode

2.1.2 Sub (System Register) Address

Sub address (System Register address) has 8-bit address space and all system registers are 8-bit data length. At multi-byte read/write transaction both I2C and SPI interface, system register address increases by 1 automatically. Brief system register map is shown as follows:

System register address	Description	Bit Assignment								Init. Value
		[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	
0x00	Audio Source On/Off	MSport0	onPort1	onPort0	onAR	onAL	onDV	onDR	onDL	0x00
0x01	Power down and mute	PD	0	0	mute	muteTime[1:0]		mclrTime[1:0]		0x80
0x02	Port0 configuration	selPCM	align[1:0]		selStereo	selMuA	compand	wlen[1:0]		0x00
0x03	Port1 configuration	selPCM	align[1:0]		selStereo	selMuA	compand	wlen[1:0]		0x00
0x04	Input Mixer Gain for left channel	sign	Gain_L_port0_left[6:0]							0x30
0x05		sign	Gain_L_port0_right[6:0]							0x60
0x06		sign	Gain_L_port1_left[6:0]							0x60
0x07		sign	Gain_L_port1_right[6:0]							0x60
0x08	Input Mixer Gain for right channel	sign	Gain_R_port0_left[6:0]							0x60
0x09		sign	Gain_R_port0_right[6:0]							0x30
0x0A		sign	Gain_R_port1_left[6:0]							0x60
0x0B		sign	Gain_R_port1_right[6:0]							0x60
0x0C	Input Mixer Gain for voice channel	sign	Gain_V_port0_left[6:0]							0x60
0x0D		sign	Gain_V_port0_right[6:0]							0x60
0x0E		sign	Gain_V_port1_left[6:0]							0x30
0x0F		sign	Gain_V_port1_right[6:0]							0x60
0x10	EQ On/Off	onGblEQ	onEQ[6:0]							0x00
0x11	Tone and Etc. On/Off	onTRBcustom	onBAScustom	0	0	onLC	onDE	onTRB	onBAS	0x00

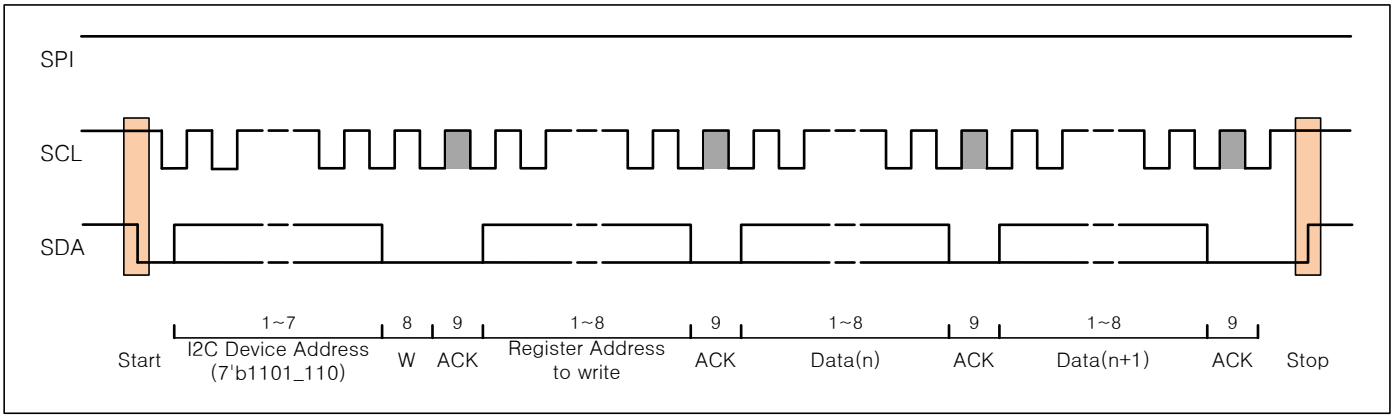
0x12	Gain of EQ1 and EQ0	gainEQ1[3:0]				gainEQ0[3:0]			0x66
0x13	Gain of EQ3 and EQ2	gainEQ3[3:0]				gainEQ2[3:0]			0x66
0x14	Gain of EQ5 and EQ4	gainEQ5[3:0]				gainEQ4[3:0]			0x66
0x15	Gain of EQ6	1	1	1	1	gainEQ6[3:0]			0xF6
0x16	Gain of Treble and Bass	gainTreble[3:0]				gainBass[3:0]			0x66
0x17	EQ custom mode On/Off	0	onEQcustom[6:0]						0x00
0x18	Coefficient0	coef0_highByte[7:0]							0x00
0x19		coef0_middleByte[7:0]							0x00
0x1A		coef0_lowByte[7:0]							0x00
0x1B	Coefficient1	coef1_highByte[7:0]							0x00
0x1C		coef1_middleByte[7:0]							0x00
0x1D		coef1_lowByte[7:0]							0x00
0x1E	Coefficient2	coef2_highByte[7:0]							0x00
0x1F		coef2_middleByte[7:0]							0x00
0x20		coef2_lowByte[7:0]							0x00
0x21	Coefficient3	coef3_highByte[7:0]							0x00
0x22		coef3_middleByte[7:0]							0x00
0x23		coef3_lowByte[7:0]							0x00
0x24	Coefficient4	coef4_highByte[7:0]							0x00
0x25		coef4_middleByte[7:0]							0x00
0x26		coef4_lowByte[7:0]							0x00
0x27	Custom filter selection	0	0	0	coefUpdate	selFilter[3:0]			0x00
0x28	AGC Configuration	onAGC	onExpand	AttackTime[5:0]					0x0E
0x29		ReleaseTime[7:0]							0x57
0x2A		Threshold[7:0]							0xB0
0x2B	3D Configuration	0	0	0	on3Dcustom	selSPK[1:0]	3Dmode	on3D	0x00
0x2C		0	CenterLev_3D[2:0]			Level_3D[3:0]			0x5A
0x2D	Digital left ch. volume	volDL[7:0]							0x58
0x2E	Digital right ch. volume	volDR[7:0]							0x58
0x2F	Digital voice ch. volume	volDV[7:0]							0x58
0x30	Dithering Configuration	0	0	0	0	enOph	enDTH	amtDTH[1:0]	0x08
0x31	PLL Configuration	PLL_Config0[7:0]							0x00
0x32		0	0	PLL_Config1[5:0]					0x00
0x33	Reserved	0	0	0	0	0	0	0 freqOSC	0x00
0x34	Analog Audio source Config.	0	0	0	0	Mono	preGain[1:0]	selAux	0x00
0x35	Analog left/right volume	0	0	volA[5:0]					0x08
0x36	Output mix for line out	mixLOR[3:0]				mixLOL[3:0]			0x44
0x37	Output mix for stereo Amp.	mixSTR[3:0]				mixSTL[3:0]			0x44
0x38	Output mix for ear Amp.	0	0	0	mixESPK[4:0]				0x10
0x39	Adj. Gain of line out	0	gainLOR[2:0]			0	gainLOL[2:0]		0x00
0x3A	Adj. Gain of loud speaker	0	gainSPKR[2:0]			0	gainSPKL[2:0]		0x00

0x3B	Adj. Gain of headphone	0	gainHPR[2:0]			0	gainHPL[2:0]			0x11
0x3C	Adj. Gain of ear speaker	selfFlt	zeroCross	VHLDO[1:0]		iovddctrl	gainESPK[2:0]			0x00
0x3D	Power amplifier On/Off	onESPK	onVCOM	onHPR	onHPL	paraSPK	onSPKR	onSPKL	onLO	0x00
0x3E	Miscellaneous Configuration	0	selDCHR	onOT	onOC	DT_ESPK[1:0]		DT_SPK[1:0]		0x00
0x3F	Clock Configuration	selCKOB[3:0]				selXtal	0	onCKOB	onCKOA	0x00
0x40	Port0 status monitoring	lock0	fs_port0[14:8]							Read Only
0x41		fs_port0[7:0]								
0x42	Port1 status monitoring	lock1	fs_port1[14:8]							
0x43		fs_port1[7:0]								
0x44	Fault Status	-	-	-	-	hPsel	fault	faultOT	faultOC	

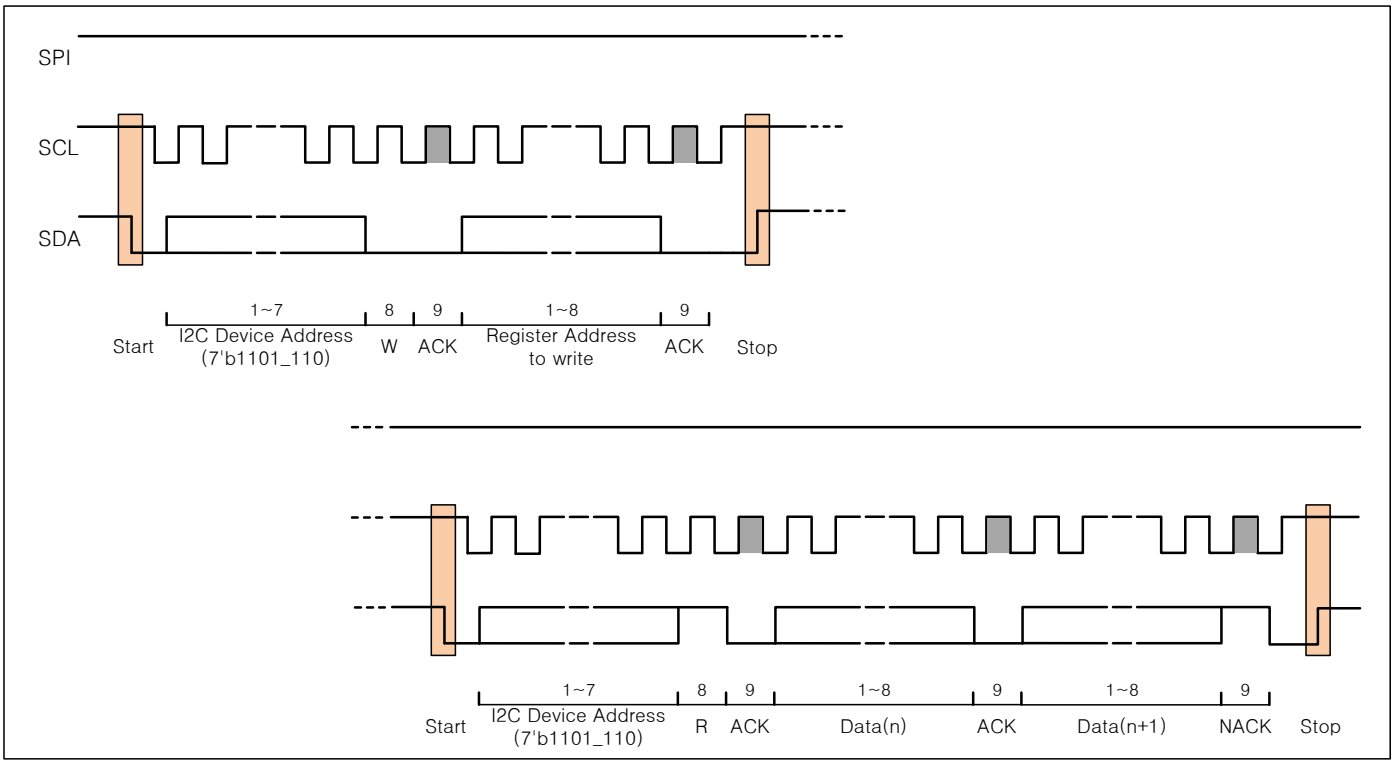
Note : 0, 1 Reserved bits. These bits must be configured like those values for normal operation.

2.2. I2C Interface

At I2C control interface, both read and write modes are available. SPI must be always high for I2C interface because SPI is low-active chip-select signal at SPI interface. I2C device address is 7'b1101_110x(0xDC). In write mode, the first write address is pointed by register address. And the next write address increases by one internally. In read mode, the first read address is pointed by register address. And the next read address increases by one internally.



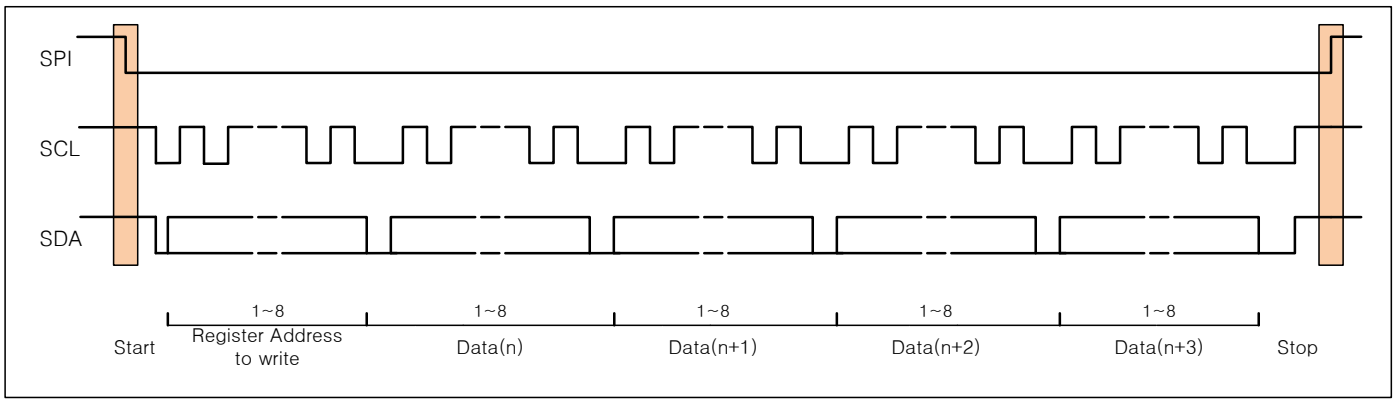
<I2C Write mode>



<I2C Read mode>

2.3. SPI Interface

At SPI control interface, only write mode is available. SPI is low-active chip-select signal, therefore falling-edge of SPI is start signal and rising-edge is end signal of SPI transaction. The first address is pointed by register address. And the next write address increases by one internally.



<SPI Write mode>

3. System Register Description

Audio Source On and Off / Address 0x00				
Bit	**Name**	**Description**	**Init. Value**	
[0]	onDL	On/Off of internal digital left channel 0:Off 1:On	0	0x00
[1]	onDR	On/Off of internal digital right channel 0:Off 1:On	0	
[2]	onDV	On/Off of internal digital voice channel 0:Off 1:On	0	
[3]	onAL	On/Off of internal analog left channel 0:Off 1:On	0	
[4]	onAR	On/Off of internal analog right channel 0:Off 1:On	0	
[5]	onPort0	On/Off of serial audio interface port0 0:Off 1:On	0	
[6]	onPort1	On/Off of serial audio interface port1 0:Off 1:On	0	
[7]	MSport0	Master/Slave configuration of serial port0 0:Slave 1:Master At slave mode, all LRCK0/SCK0/SD0 of port0 are input. At master mode, all LRCK0/SCK0/SD0 of port0 are output, and sample-rate-converted data (fs=48kHz) of port1 serial audio data is uploaded by I2S interface to port0 pins.	0	

Power Down and Mute / Address 0x01				
Bit	**Name**	**Description**	**Init. Value**	
[1:0]	mclrTime[1:0]	Mute clear time for soft mute clear At digital volume, 00:21us/0.25dB, 01:0.67ms/0.25dB, 10:1.33ms/0.25dB, 11:2.67ms/0.25dB At analog volume, 00:31us/2dB, 01:4ms/2dB, 10:8ms/2dB, 11:16ms/2dB	00	0x80
[3:2]	muteTime[1:0]	Mute time for soft mute At digital volume, 00:21us/0.25dB, 01:0.67ms/0.25dB, 10:1.33ms/0.25dB, 11:2.67ms/0.25dB At analog volume, 00:31us/2dB, 01:4ms/2dB, 10:8ms/2dB, 11:16ms/2dB	00	
[4]	mute	On/Off of Mute 0:Mute Clear 1:Mute On	0	
[6:5]	Reserved	Reserved, must be “00”.	00	
[7]	PD	Software power down. 0:Nomal operation 1:Power Down	1	

Serial Port0 Configuration / Address 0x02				
Bit	**Name**	**Description**	**Init. Value**	
[1:0]	wlen[1:0]	Serial data word length of port0. At I2S compatible interface, 00:24-bit, 01:20-bit, 10:18-bit, 11:16bit At PCM interface, 00:16-bit, 01:13-bit, 10:12-bit, 11:8-bit	00	0x00
[2]	compand	Selection of compand mode of port0. This bit is valid at PCM 8-bit mode. 0:Not compand(linear PCM) 8-bit PCM data, 1:compand 8-bit PCM data	0	

[3]	selMuA	Selection of u-law/A-law compand of port0. This bit is valid at compand 8-bit PCM. 0:A-law compand, 1:u-law compand	0	
[4]	selStereo	Selection of stereo 8-bit PCM mode of port0. This bit is valid at 8-bit PCM mode. 0:Mono 8-bit PCM data, 1:Stereo 8-bit PCM data	0	
[6:5]	align[1:0]	Selection of serial data alignment of port0. At I2S compatible mode, 00:I2S align, 01:Left-justfied, 10:Rignt-justfied At PCM mode, 01:Left-justfied, 10:Right-justfied	00	
[7]	selPCM	Selection of serial audio input interface of port0. 0:I2S compatible interface 1:PCM interface Short-frame / long-frame PCM interfaces are auto-detected.	0	

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Serial Port1 Configuration / Address 0x03				
Bit	**Name**	**Description**	**Init. Value**	
[1:0]	wlen[1:0]	Serial data word length of port1. At I2S compatible interface, 00:24-bit, 01:20-bit, 10:18-bit, 11:16bit At PCM interface, 00:16-bit, 01:13-bit, 10:12-bit, 11:8-bit	00	0x00
[2]	compand	Selection of compand mode of port1. This bit is valid at PCM 8-bit mode. 0:Not compand(linear PCM) 8-bit PCM data, 1:compand 8-bit PCM data	0	
[3]	selMuA	Selection of u-law/A-law compand of port1. This bit is valid at compand 8-bit PCM. 0:A-law compand, 1:u-law compand	0	
[4]	selStereo	Selection of stereo 8-bit PCM mode of port1. This bit is valid at 8-bit PCM mode. 0:Mono 8-bit PCM data, 1:Stereo 8-bit PCM data	0	
[6:5]	align[1:0]	Selection of serial data alignment of port1. At I2S compatible mode, 00:I2S align, 01:Left-justfied, 10:Rignt-justfied At PCM mode, 01:Left-justfied, 10:Right-justfied	00	
[7]	selPCM	Selection of serial audio input interface of port1. 0:I2S compatible interface 1:PCM interface Short-frame / long-frame PCM interfaces are auto-detected.	0	

Mixing Gain of port0_left into internal Left channel / Address 0x04				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_L port0_left	Mixing Gain of port0_left into internal Left channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x30	0x30
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port0_right into internal Left channel / Address 0x05				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_L port0_right	Mixing Gain of port0_right into internal Left channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port1_left into internal Left channel / Address 0x06				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_L port1_left	Mixing Gain of port1_left into internal Left channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port1_right into internal Left channel / Address 0x07				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_L port1_right	Mixing Gain of port1_right into internal Left channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port0_left into internal Right channel / Address 0x08				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_R port0_left	Mixing Gain of port0_left into internal Right channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port0_right into internal Right channel / Address 0x09				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_R port0_right	Mixing Gain of port0_right into internal Right channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x30	0x30
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port1_left into internal Right channel / Address 0x0A				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_R port1_left	Mixing Gain of port1_left into internal Right channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port1_right into internal Right channel / Address 0x0B				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_R port1_right	Mixing Gain of port1_right into internal Right channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port0_left into internal Voice channel / Address 0x0C				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_V port0_left	Mixing Gain of port0_left into internal Voice channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port0_right into internal Voice channel / Address 0x0D				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_V port0_right	Mixing Gain of port0_right into internal Voice channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port1_left into internal Voice channel / Address 0x0E				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_V port1_left	Mixing Gain of port1_left into internal Voice channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x30	0x30
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Mixing Gain of port1_right into internal Voice channel / Address 0x0F				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	Gain_V port1_right	Mixing Gain of port1_right into internal Voice channel Mixing range is +24~-23.5dB, -∞, 0.5dB step. Appendix C shows register value of mixer gain.	0x60	0x60
[7]	sign	Sign of mixing gain. 0:Plus (positive phase), 1:Minus(negative phase)	0	

Equalizer On and Off / Address 0x10				
Bit	**Name**	**Description**	**Init. Value**	
[0]	onEQ0	On/Off EQ0. To turn-on EQ0, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	0x00
[1]	onEQ1	On/Off EQ0. To turn-on EQ1, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	
[2]	onEQ2	On/Off EQ0. To turn-on EQ2, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	
[3]	onEQ3	On/Off EQ0. To turn-on EQ3, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	
[4]	onEQ4	On/Off EQ0. To turn-on EQ4, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	

[5]	onEQ5	On/Off EQ0. To turn-on EQ5, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	
[6]	onEQ6	On/Off EQ0. To turn-on EQ6, both onGblEQ(0x10.[7]) and onEQ0 must be set. Center freq. : 63Hz, Q:1.0, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	
[7]	onGblEQ	Global On/Off of 7-band equalizer. 0:Global Off, 1:Global On	0	

Tone and Etc. On and Off / Address 0x11				
Bit	**Name**	**Description**	**Init. Value**	
[0]	onBAS	On/Off of Bass (Tone control) Center freq. : 150Hz, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	0x00
[1]	onTRB	On/Off of Treble (Tone control) Center freq. : 7kHz, gain range:+12~-12dB/2dB step 0:Off, 1:On	0	
[2]	onDE	On/Off of Deemphasis. 0:Off, 1:On	0	
[3]	onLC	On/Off of Loudness compensation. 0:Off, 1:On	0	
[5:4]	Reserved	Reserved, must be "00".	00	
[6]	onBAScustom	On/Off of Bass custom mode. 0: Off, 1:On In case the internal coefficients of Bass filter are not proper, a new appropriate coefficient set can be downloaded into this chip through I2C/SPI interface. After completion of download, Bass custom mode can be turn-on to operate the filter with the new coefficient set.	0	
[7]	onTRBcustom	On/Off of Treble custom mode. 0: Off, 1:On In case the internal coefficients of Treble filter are not proper, a new appropriate coefficient set can be downloaded into this chip through I2C/SPI interface. After completion of download, Treble custom mode can be turn-on to operate the filter with the new coefficient set.	0	

Gain of EQ1 and EQ0 / Address 0x12				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	gainEQ0[3:0]	Selection of EQ0 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	0x66
[7:4]	gainEQ1[3:0]	Selection of EQ1 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	

Gain of EQ3 and EQ2 / Address 0x13				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	gainEQ2[3:0]	Selection of EQ2 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	0x66
[7:4]	gainEQ3[3:0]	Selection of EQ3 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	

Gain of EQ5 and EQ4 / Address 0x14				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	gainEQ4[3:0]	Selection of EQ4 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	0x66
[7:4]	gainEQ5[3:0]	Selection of EQ5 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	

Gain of EQ6 / Address 0x15				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	gainEQ6[3:0]	Selection of EQ6 gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	0xF6
[7:4]	Reserved	Reserved, must be "1111".	1111	

Gain of Bass and Treble / Address 0x16				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	gainBass[3:0]	Selection of Bass gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	0x66
[7:4]	gainTreble[3:0]	Selection of Treble gain Range of gain +12 ~ -12dB / 2dB step. Appendix D shows register value of filter gain.	0110	

EQ custom mode On and Of / Address 0x17				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	onEQcustom [6:0]	On/Off of EQ custom mode. [0]:On/Off EQ0 custom mode [1]:On/Off EQ1 custom mode [2]:On/Off EQ2 custom mode [3]:On/Off EQ3 custom mode [4]:On/Off EQ4 custom mode [5]:On/Off EQ5 custom mode [6]:On/Off EQ6 custom mode 0:Off, 1:On In case the internal coefficients of EQx filter are not proper, a new appropriate coefficient set can be downloaded into this chip through I2C/SPI interface. After completion of download, EQx custom mode can be turn-on to operate filter with the new coefficient set.	0x00	0x00
[7]	Reserved	Reserved, must be "0".	0	

High byte of Coefficient 0 / Address 0x18				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef0_highByte [7:0]	High byte register of coefficient 0. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Middle byte of Coefficient 0 / Address 0x19				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef0_midByte [7:0]	Middle byte register of coefficient 0. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Low byte of Coefficient 0 / Address 0x1A				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef0_lowByte [7:0]	Low byte register of coefficient 0. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

High byte of Coefficient 1 / Address 0x1B				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef1_highByte [7:0]	High byte register of coefficient 1. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Middle byte of Coefficient 1 / Address 0x1C				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef1_midByte [7:0]	Middle byte register of coefficient 1. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Low byte of Coefficient 1 / Address 0x1D				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef1_lowByte [7:0]	Low byte register of coefficient 1. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

High byte of Coefficient 2 / Address 0x1E				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef2_highByte [7:0]	High byte register of coefficient 2. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Middle byte of Coefficient 2 / Address 0x1F				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef2_midByte [7:0]	Middle byte register of coefficient 2. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Low byte of Coefficient 2 / Address 0x20				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef2_lowByte [7:0]	Low byte register of coefficient 2. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

High byte of Coefficient 3 / Address 0x21				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef3_highByte [7:0]	High byte register of coefficient 3. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Middle byte of Coefficient 3 / Address 0x22				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef3_midByte [7:0]	Middle byte register of coefficient 3. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Low byte of Coefficient 3 / Address 0x23				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef3_lowByte [7:0]	Low byte register of coefficient 3. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

High byte of Coefficient 4 / Address 0x24				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef4_highByte [7:0]	High byte register of coefficient 4. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Middle byte of Coefficient 4 / Address 0x25				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef4_midByte [7:0]	Middle byte register of coefficient 4. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Low byte of Coefficient 4 / Address 0x26				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	coef4_lowByte [7:0]	Low byte register of coefficient 4. Coefficient 0 consists of 3-byte(24-bit/3.21-format) high-byte, mid-byte and low-byte.	0x00	0x00

Custom Filter Selection and Coefficient Update / Address 0x27				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	selFilter[7:0]	Selection of filter to be made to customize filter. 0000:EQ0 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0001:EQ1 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0010:EQ2 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0011:EQ3 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0100:EQ4 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0101:EQ5 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0110:EQ6 bi-quad filter coef.{b0 b1 b2 –a1 –a2} 0111:Bass 1st oder IIR filter coef.{b0 b1 -a1} 1000:Treble 1st oder IIR filter coef.{b0 b1 -a1} 1001:3D left0 left ch. 7th order IIR filter coef.{b0 b1 b2 b3 b4} 1010:3D left1 left ch. 7th order IIR filter coef.{b5 b6 b7 –a1 –a2}	0000	0x00

		1011:3D left2 left ch. 7th order IIR filter coef.{–a3 –a4 –a5 –a6 –a7} 1100:right0 left ch. 7th order IIR filter coef.{b0 b1 b2 b3 b4} 1101:right1 left ch. 7th order IIR filter coef.{b0 b1 b2 b3 b4} 1110:right2 left ch. 7th order IIR filter coef.{–a3 –a4 –a5 –a6 –a7}		
[4]	coefUpdate	Coefficient update signal. 0:update disable, 1:update by rising edge of this bit After the completion of coefficient transmit, this bit must be set, and reset again for next coef. update cycle. If this bit is set(really rising edge of this bit), coefficients in coef0 /coef1/coef2/coef3/coef4 registers are moved to corresponding coefficient memory of the selected filter by "selFilter[3:0]". If coef. update is completed, then custom mode of the corresponding filter can be turn-on.	0	
[7:5]	Reserved	Reserved, must be "000".	000	

AGC Mode and Attack Time / Address 0x28				
Bit	**Name**	**Description**	**Init. Value**	
[5:0]	AttackTime [5:0]	Selection of AGC attack time. Resolution of attack time is 21us/0.25dB(resolution of τ=0.7ms/8.68dB) Attack time = AttackTime[5:0] * 21us Timer constant(τ) of attack time = AttackTime[5:0] * 0.7ms Appendix F shows register value of attack time of AGC.	0x0E	0x0E
[6]	onExpand	On/Off of AGC Expand mode. 0:AGC expand Off, 1:AGC expand On	0	
[7]	onAGC	On/Off AGC mode. 0:AGC Off, 1:AGC On At AGC mode, there are two modes; one is AGC expand mode and the other is AGC not-expand mode. At AGC not-expand mode, internal volume is auto-controlled to limit the peak value of audio signal to threshold of AGC; that is, if peak level of audio is high, internal volume is adjusted down, and if peak value of audio is low, then boosted up to the threshold level. In order to turn-on AGC expand, turn-on both onAGC(0x27.[7]) and onExpand.	0	

AGC Release Time / Address 0x29				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	ReleaseTime [7:0]	Selection of AGC release time. Resolution of release time is 333us/0.25dB(resolution of τ==11.6ms/8.68dB) Release time = ReleaseTime[7:0] * 11.6ms Appendix G shows register value of release time of AGC.	0x57	0x57

AGC Threshold Level/ Address 0x2A				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	Threshold [7:0]	Selection of AGC threshold. Resolution of release time is 333us/0.25dB(resolution of τ==11.6ms/8.68dB) Appendix H shows register value of threshold level of AGC.	0xB0	0xB0

3D Mode / Address 0x2B				
Bit	**Name**	**Description**	**Init. Value**	
[0]	on3D	On/Off of stereo 3D function. 0:Off, 1:On	0	0x00
[1]	3Dmode	Selection of 3D mode. 0:Loud speaker mode, 1:Headphone mode	0	
[3:2]	selSPK[1:0]	Selection of angle between stereo speakers. This bit is valid at Loud speaker 3D mode(3Dmode=low). 00:angle≤5°, 01: 5°≤angle≤20°, 10:20°<angle	00	
[7:4]	Reserved	Reserved, must be "0000".	0000	

3D Level / Address 0x2C				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	Level_3D[3:0]	Selection of 3D level. At 3D loud speaker mode, 0000:0.0, 0001:0.1, 0010:0.2, 0011:0.3, 0100:0.4, 0101:0.5 0110:0.6, 0111:0.7, 1000:0.8, 1001:0.9, 1010:1.0 At 3D headphone mode, 0000:0.0, 0001:0.1, 0010:0.2, 0011:0.3, 0100:0.4, 0101:0.5 0110:0.6, 0111:0.7, 1000:0.8, 1001:0.9, 1010:1.0, 1011:1.1 1100:1.2, 1101:1.3, 1110:1.4	1010	0x5A
[6:4]	CenterLev_3D [2:0]	Selection of Center level of 3D speaker mode. These bits are valid at 3D speaker mode, and determines the sound level of virtual center position. 000:-16dB attenuation 001:-17dB attenuation 010:-18dB attenuation 011:-19dB attenuation 100:-20dB attenuation 101:-∞ attenuation	101	
[7]	Reserved	Reserved, must be "0".	0	

Digital Left Channel Volume / Address 0x2D				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	volDL[7:0]	Selection of digital left channel volume. Volume range is +24~-75dB,-∞ / basically 0.5dB variable step. Resolution of soft-volume is 0.25dB by using interpolation of volume table. Appendix A shows the register value of digital volume.	0x58	0x58

Digital Right Channel Volume / Address 0x2E				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	volDR[7:0]	Selection of digital Right channel volume. Volume range is +24~-75dB,-∞ / basically 0.5dB variable step. Resolution of soft-volume is 0.25dB by using interpolation of volume table. Appendix A shows the register value of digital volume.	0x58	0x58

Digital Voice Channel Volume / Address 0x2F				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	volDV[7:0]	Selection of digital voice channel volume. Volume range is +24~-75dB,-∞ / basically 0.5dB variable step. Resolution of soft-volume is 0.25dB by using interpolation of volume table. Appendix A shows the register value of digital volume.	0x58	0x58

Dithering / Address 0x30				
Bit	**Name**	**Description**	**Init. Value**	
[1:0]	amtDTH[1:0]	Selection of dither level. 00:-108dB(18-bit), 01:-102dB(17-bit), 10:-96dB(16-bit), 11:-90dB(15-bit)	00	0x08
[2]	enDTH	On/Off of dithering function 0:Off, 1:On	0	
[3]	enOph	On/Off of PWM out-of-phase function. 0:pwm out-of-phase Off, 1:pwm out-of-phase On	1	
[7:4]	Reserved	Reserved, must be "0000".	0000	

PLL Configuration 0 / Address 0x31				
Bit	**Name**	**Description**	**Init. Value**	
[5:0]	P[5:0]	Selection of post divider of PLL. Fout = M*Fin/(8*P*S), where M:M[5:0]value, P:P[5:0] value, S:S[1:0] value	0x00	0x00
[7:6]	S[1:0]	Selection of prescaler of PLL. Fout = M*Fin/(8*P*S), where M:M[5:0]value, P:P[5:0] value, S:S[1:0] value	00	

PLL Configuration 1 / Address 0x32				
Bit	**Name**	**Description**	**Init. Value**	
[5:0]	M[5:0]	Selection of post divider of PLL. Fout = M*Fin/(8*P*S), where M:M[5:0]value, P:P[5:0] value, S:S[1:0] value	0x00	0x00
[7:6]	Reserved	Reserved, must be "00".	00	

Charge Pump Configuration / Address 0x33				
Bit	**Name**	**Description**	**Init. Value**	
[0]	freqOSC	Selection of frequency of charge-pump 0: 500kHz, 1: 700kHz	0	0x00
[7:1]	Reserved	Reserved, must be "00".	0x00	

Analog Audio Source Configuration/ Address 0x34				
Bit	**Name**	**Description**	**Init. Value**	
[0]	selAux	Selection of analog audio source. 0:AUXL1, AUXR1 selected, 1:AUXL2,AUXR2 selected	0	0x00
[2:1]	preGain[1:0]	Selection of pre-amplifier gain of analog audio source. 00:0dB, 01:+6dB, 10:+12dB, 11:+18dB	00	
[3]	Mono	Selection of differential input between AUXL and AUXR 0:Single-ended input 1:Differential input(AUXL:positive input pin, AUXR:negative input pin)	0	
[7:4]	Reserved	Reserved, must be "0000".	0000	

Analog Left/Right Volume / Address 0x35				
Bit	**Name**	**Description**	**Init. Value**	
[5:0]	volA[5:0]	Selection of analog left/right channel volume. Volume range:+16~-72dB, -∞/2dB step Resolution of soft-volume is 2dB by using analog volume table. Appendix B shows the register value of analog volume.	0x08	0x08
[7:6]	Reserved	Reserved, must be "00".	00	

Output Mixer for Line Out / Address 0x36				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	mixLOL[3:0]	Mixer On/Off for line out left channel. 0:Off, 1:On [0]:Analog left channel switch [1]:Analog right channel switch [2]:Digital left channel switch [3]:Digital right channel switch	0100	0x44
[7:4]	mixLOR[3:0]	Mixer On/Off for line out right channel. 0:Off, 1:On [0]:Analog left channel switch [1]:Analog right channel switch [2]:Digital left channel switch [3]:Digital right channel switch	0100	

Output Mixer for Stereo Amplifier / Address 0x37				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	mixSTL[3:0]	Mixer On/Off for stereo left channel. 0:Off, 1:On [0]:Analog left channel switch [1]:Analog right channel switch [2]:Digital left channel switch [3]:Digital right channel switch	0100	0x44
[7:4]	mixSTR[3:0]	Mixer On/Off for stereo right channel. 0:Off, 1:On [0]:Analog left channel switch [1]:Analog right channel switch [2]:Digital left channel switch [3]:Digital right channel switch	0100	

Output Mixer for Mono Ear Speaker Amplifier / Address 0x38				
Bit	**Name**	**Description**	**Init. Value**	
[3:0]	mixESPK[4:0]	Mixer On/Off for ear speaker amplifier channel. 0:Off, 1:On [0]:Analog left channel switch [1]:Analog right channel switch [2]:Digital left channel switch [3]:Digital right channel switch	0x10	0x10
[7:5]	Reserved	Reserved, must be "000".	000	

Adjustable Gain of Line Out / Address 0x39				
Bit	**Name**	**Description**	**Init. Value**	
[2:0]	gainLOL[2:0]	Selection of adjustable attenuation gain of line out left channel. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	0x00
[3]	Reserved	Reserved, must be"0".	0	
[6:4]	gainLOR[2:0]	Selection of adjustable attenuation gain of line out right channel. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	
[7]	Reserved	Reserved, must be "0".	0	

Adjustable Gain of Loud Speaker Amplifier / Address 0x3A				
Bit	**Name**	**Description**	**Init. Value**	
[2:0]	gainSPKL[2:0]	Selection of adjustable attenuation gain of speaker amplifier left channel. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	0x00
[3]	Reserved	Reserved, must be"0".	0	
[6:4]	gainSPKR[2:0]	Selection of adjustable attenuation gain of speaker amplifier right channel. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	
[7]	Reserved	Reserved, must be "0".	0	

Adjustable Gain of Headphone Amplifier / Address 0x3B				
Bit	**Name**	**Description**	**Init. Value**	
[2:0]	gainHPL[2:0]	Selection of adjustable attenuation gain of headphone amplifier left channel. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	0x00
[3]	Reserved	Reserved, must be"0".	0	
[6:4]	gainHPR[2:0]	Selection of adjustable attenuation gain of headphone amplifier right channel. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	
[7]	Reserved	Reserved, must be "0".	0	

Adjustable Gain of Mono Ear Speaker Amplifier and Option / Address 0x3C				
Bit	**Name**	**Description**	**Init. Value**	
[2:0]	gainESPK[2:0]	Selection of adjustable attenuation gain of mono ear speaker amplifier. 000:0dB, 001:-2dB, 010:-4dB, 011:-6dB, 100:-8dB, 101:-10dB, 110:-12dB, 111:-14dB Appendix E shows register value of adjustable gain table for power amplifiers.	000	0x00
[3]	IOvddctrl	Selection supply voltage of port0. 0:1.8V, 1:IOvdd	0	
[5:4]	VHLDO	Selection of headphone amplifier power(LDO output) 00: 2.5V, 01: 2.2V, 10: 1.9V, 11:1.6V	00	
[6]	zeroCross	Selection of zero-crossing to suppress pop-noise 0:enable, 1:disable	0	
[7]	selfFlt	Selection of Fault recovery to automate. 0:disable, 1:enable	0	

Power Amp On and Off / Address 0x3D				
Bit	**Name**	**Description**	**Init. Value**	
[0]	onLO	On/Off of line out left/right channel. 0:Off, 1:On	0	0x00
[1]	onSPKL	On/Off of loud speaker amplifier left channel. 0:Off, 1:On	0	
[2]	onSPKR	On/Off of loud speaker amplifier right channel. 0:Off, 1:On	0	

[3]	paraSPK	Selection of parallel configuration of stereo loud speaker amplifier to support 4Ω load. 0:Stereo mode, 1:Parallel mode At parallel mode, SPKLA and SPKRA are tied, SPKLB and SPKRB are tied. At parallel mode, only left channel signal is played.	0	
[4]	onHPL	On/Off of headphone amplifier left channel. 0:Off, 1:On	0	
[5]	onHPR	On/Off of headphone amplifier right channel. 0:Off, 1:On	0	
[6]	onVCOM	On/Off of virtual ground amplifier for DC-blocking cap-less headphone application. The virtual ground is center voltage of power supply voltage. 0:Off, 1:On	0	
[7]	onESPK	On/Off of mono ear speaker amplifier 0:Off, 1:On	0	

Miscellaneous Configuration / Address 0x3E				
Bit	**Name**	**Description**	**Init. Value**	
[1:0]	DT_SPK[1:0]	Selection of dead time of stereo loud speaker amplifier. 00:1.2ns, 01:2.4ns, 10:3.6ns, 11:4.8ns	0	0x00
[3:2]	DT_ESPK[1:0]	Selection of dead time of mono ear speaker amplifier. 00:1.2ns, 01:2.4ns, 10:3.6ns, 11:4.8ns	0	
[4]	onOC	On/Off of over current protection. 0:Off, 1:On	0	
[5]	onOT	On/Off of over temperature protection. 0:Off, 1:On	0	
[6]	selDCHR	Selection of discharging resister of DC-blocking capacitor of headphone connection. This bit is "don't care" at DC-blocking cap-less application. 0:DC-blocking capacitor, Cdc≤47uF 1:DC-blocking capacitor, Cdc>47uF	0	
[7]	Reserved	Reserved, must be "0".	0	

X-tal ,Clock In and Out / Address 0x3F				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	Reserved	Reserved	0	0x00

Port0 Status(Read only) / Address 0x40				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	fs_port0[14:8]	Sample Frequency[14:8] status of port0 Sample Frequency of port0 = fs_port[14:8]*48/2*2^{-12} If fs0=48kHz, then fs_port0[14:0]=0x2000 If fs0=44.1kHz, then fs_port0[14:0]=0x1D66 If fs0=32kHz, then fs_port0[14:0]=0x1555 If fs0=16kHz, then fs_port0[14:0]=0x0AAB If fs0=8kHz, then fs_port0[14:0]=0x0555	-	Read Only
[7]	Lock0	Locking status of port0 0:Locking fail, 1:Locking	-	

Port0 Status(Read only) / Address 0x41				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	fs_port0[7:0	Sample Frequency[14:8] status of port0 Sample Frequency of port0 = fs_port[14:8]*48/2*2^{-12}[kHz] If fs0=48kHz, then fs_port0[14:0]=0x2000 If fs0=44.1kHz, then fs_port0[14:0]=0x1D66 If fs0=32kHz, then fs_port0[14:0]=0x1555 If fs0=16kHz, then fs_port0[14:0]=0x0AAB If fs0=8kHz, then fs_port0[14:0]=0x0555	-	Read Only

Port1 Status(Read only) / Address 0x42				
Bit	**Name**	**Description**	**Init. Value**	
[6:0]	fs_port1[14:8]	Sample Frequency[14:8] status of port0 Sample Frequency of port1 = fs_port[14:8]*48/2*2^{-12}[kHz] If fs1=48kHz, then fs_port1[14:0]=0x2000 If fs1=44.1kHz, then fs_port1[14:0]=0x1D66 If fs1=32kHz, then fs_port1[14:0]=0x1555 If fs1=16kHz, then fs_port1[14:0]=0x0AAB If fs1=8kHz, then fs_port1[14:0]=0x0555	-	Read Only
[7]	Lock0	Locking status of port0 0:Locking fail, 1:Locking	-	

Port1 Status(Read only) / Address 0x43				
Bit	**Name**	**Description**	**Init. Value**	
[7:0]	fs_port1[14:8]	Sample Frequency[14:8] status of port0 Sample Frequency of port1 = fs_port[14:8]*48/2*2^{3}[kHz] If fs1=48kHz, then fs_port1[14:0]=0x2000 If fs1=44.1kHz, then fs_port1[14:0]=0x1D66 If fs1=32kHz, then fs_port1[14:0]=0x1555 If fs1=16kHz, then fs_port1[14:0]=0x0AAB If fs1=8kHz, then fs_port1[14:0]=0x0555	-	Read Only

Fault and Headphone Status(Read Only) / Address 0x44				
Bit	**Name**	**Description**	**Init. Value**	
[0]	faultOC	Over current fault status 0:normal, 1:over current fault detected	-	Read Only
[1]	faultOT	Over temperature fault status 0:normal, 1:over temperature fault detected		
[2]	fault	Total fault status. fault = faultOC or faultOT. 0:nomal, 1:over current or over temperature fault detected		
[3]	HPsel	Status of Headphone insertion to headphone jack 0:HPSEL\ pin is high, 1:HPSEL\ pin is low		
[7:4]	Reserved	Reserved		

4. SYSTEM FUNCTION DESCRIPTION

4.1 Power Supply

4.1.1 Power Supply for PLL

PLL is a low-jitter, programmable phase-locked loop frequency synthesizer using 0.18um CMOS process technology. DPLLVDD18 and DPLLGND pins are power supply of digital part of PLL. And APLLVDD18 and APLLGND pins are power supply of analog part of PLL.

4.1.2 Power Supply for digital core-logic

Digital core logic is based on 0.18um CMOS process technology. DVDD and DGND pins are power supply of digital core-logic.

4.1.3 Power Supply for I/O signals

I/O Power can select a variety of voltage because we don't know U-com`s power. I/O Power normally use 1.8V voltage. If you use different I/O digital voltage, you should connect different voltage to IOVDD pad and then set iovddctrl(system register 0x3C.[3]).

4.1.4 Power Supply for analog processing core

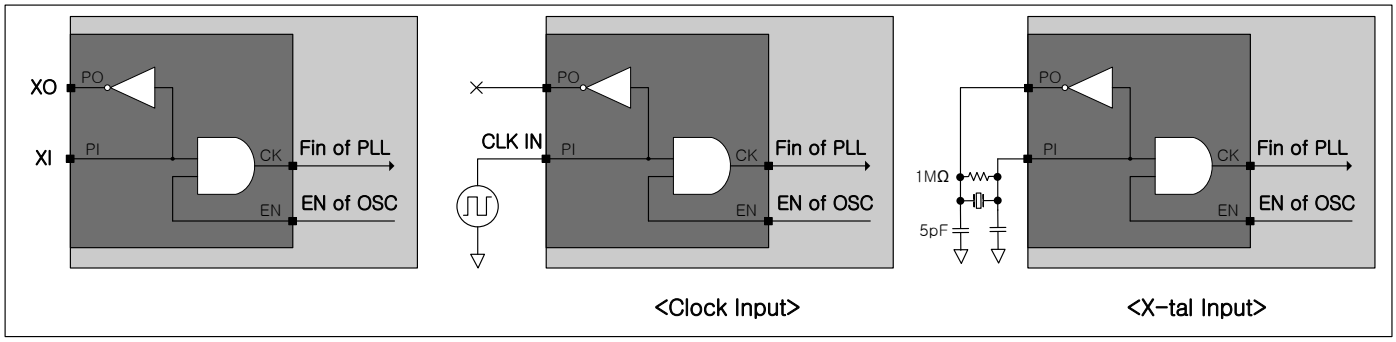
Analog processing core is based on CMOS process technology. AVDD and AGND pins are power supply of analog core.

4.1.5 Power Supply for amplifiers

Amplifiers are based on CMOS process technology. PVDD1/PVDD2 and PGND1/PGND2 pins are power supply of power amplifier. EVDD and EGND pins are power supply of mono ear speaker amplifier.

4.2 X-tal / Clock In, PLL and Clock Out

4.2.1 X-tal and Clock In



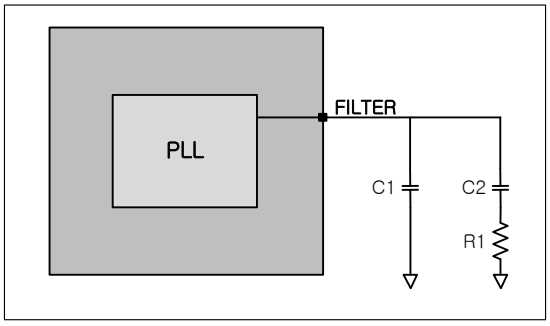
Both clock source and X-tal are supported. Available clock sources are 12 ~ 28MHz.

4.2.1 PLL

PLL is a low-jitter, programmable phase-locked loop frequency synthesizer using 0.18um CMOS process technology.
Fout = M*Fin/(8*P*S), where M:M[5:0], P:P[5:0], S:[1:0] value.
Recommended M, P and S values as input frequency are as follows:

Fin [MHz]	M[5:0]	P[5:0]	S[1:0]	Fout [MHz]
2.048	24	2	2	98.304
4.096	24	4	2	98.304
6.144	8	2	2	98.304
12.288	8	4	2	98.304
16.384	9	6	2	98.304
18.432	8	6	2	98.304
24.576	8	8	2	98.304

Recommended external loop filter is shown as follows:



Fin=16.384MHz, C1=4.7nF, C2=330pF,
R1=2.7KΩ

4.2.2 System clock, reset and power down mode

Output frequency, Fout(2048*fs, fs is internal sampling frequency.) is used as system clock of this chip. This chip is reset by low-active RESET/CPSRR external pin. Power down mode is supported by software PD (system register 0x01.[7]) through serial I2C/SPI control interface. At assertion of reset, all system registers configured by I2C/SPI interface are reset into default state, but at power down mode all system registers are maintained. Therefore after de-assertion of power down, there is no need to configure system registers again.

4.3 Audio Interface

4.3.1 General Description

It supports independent 2-port stereo digital audio signal and independent 2-port stereo analog audio signal. On/Off control bits of 2-port digital audio sources are "onPort0"(0x00.[5]) and "onPort1"(0x00.[6]). On/Off control bits of analog audio sources are "onAL"(0x00.[3]) and "onAR"(0x00.[4]). It recommended that on/off configuration of "not-used" should be "off" for low power consumption.

Supported digital audio interfaces are I2S compatible interface and PCM interface. I2S compatible interfaces are I2S, left-justified and right-justified format. PCM interfaces are short-frame and long-frame interfaces. Short-frame and long-frame of PCM interface is auto-detected, therefore there is no need to configure the short-frame of long-frame. At the PCM interface, u-law / A-law compand mode is supported and 8-bit stereo PCM interface is also supported.

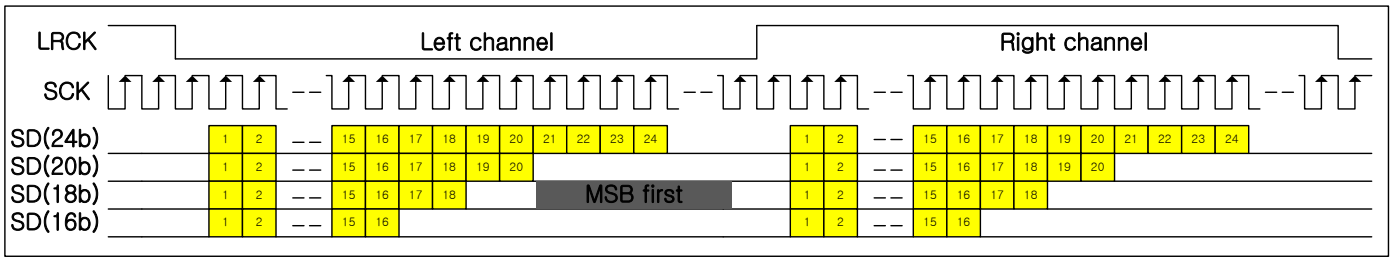
Supported sampling frequencies are 8kHz ~ 48kHz. Word length is 24/20/18/16-bit at I2S compatible interface and 16/13/12/8-bit at PCM interface. Serial data(SD) bit is valid at rising edge of serial bit clock(SCK) at I2S compatible interface. Serial data(SD) bit is valid at falling edge of serial bit clock(SCK) at PCM interface. All supported interface formats are 'MSB first' mode.

The port0 of digital audio interface can be input or output-direction by configuration of MSport(0x00.[7]). When MSport0 is low (slave mode), all pins (LRCK0/SCK0/SD0) of port0 are input-pin and when MSport0 is high (master mode), all pins of port0 are output-pin. At master mode (MSport0=high), the sample-rate-converted audio data of port1 interface is transmitted out through port0 with sampling frequency fs=48kHz and I2S interface format.

Independent 2-port stereo analog signals are selected by configuration of "selAux" (0x34[0]) signal. Single-ended left/right input pins can be configured as differential input. At the differential input mode, left channel signal pin is positive input pin and right channel signal pin is negative input pin.

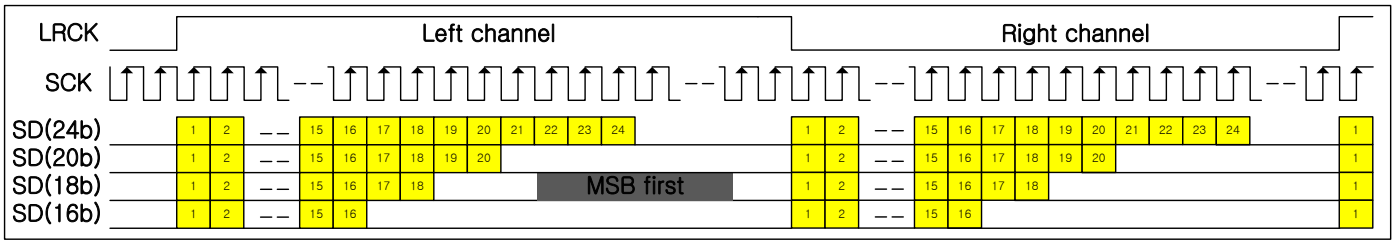
4.3.2 I2S compatible interface

▶I2S Interface format



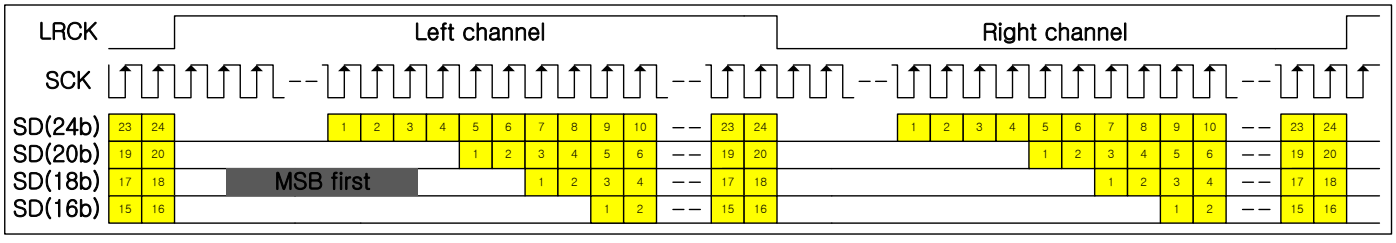
-left ch. data : when LRCK=0, right ch. data : when LRCK=1

▶Left-justified Interface format



-left ch. data : when LRCK=1, right ch. data : when LRCK=0

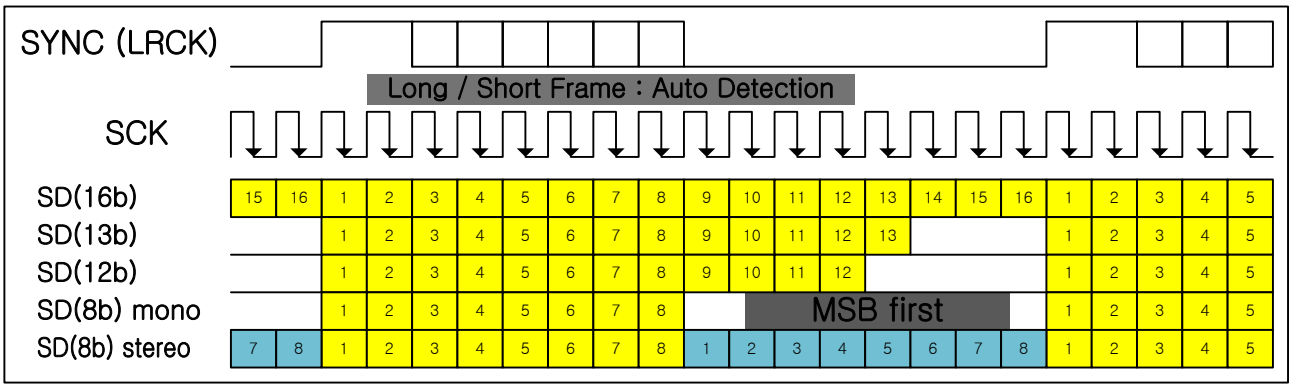
▶Right-justified Interface format



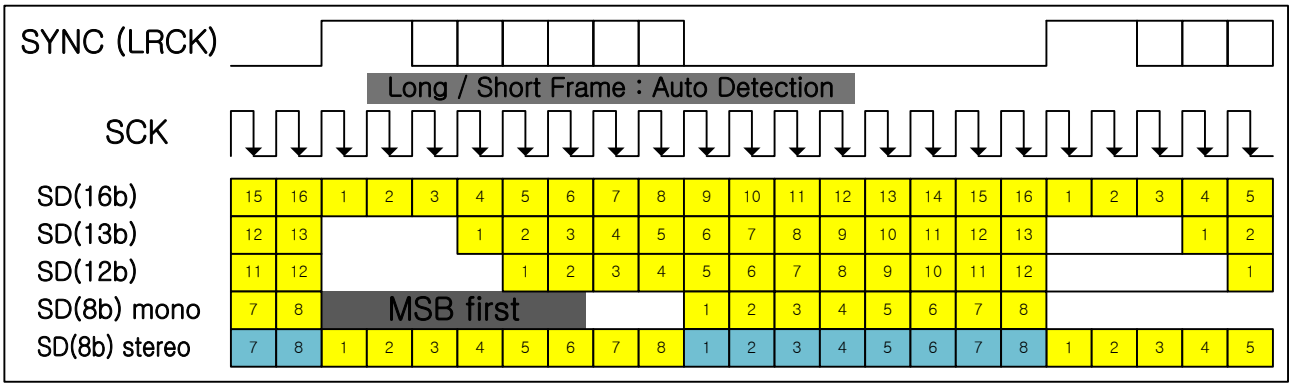
-left ch. data : when LRCK=1, right ch. data : when LRCK=0

4.3.3 PCM interface

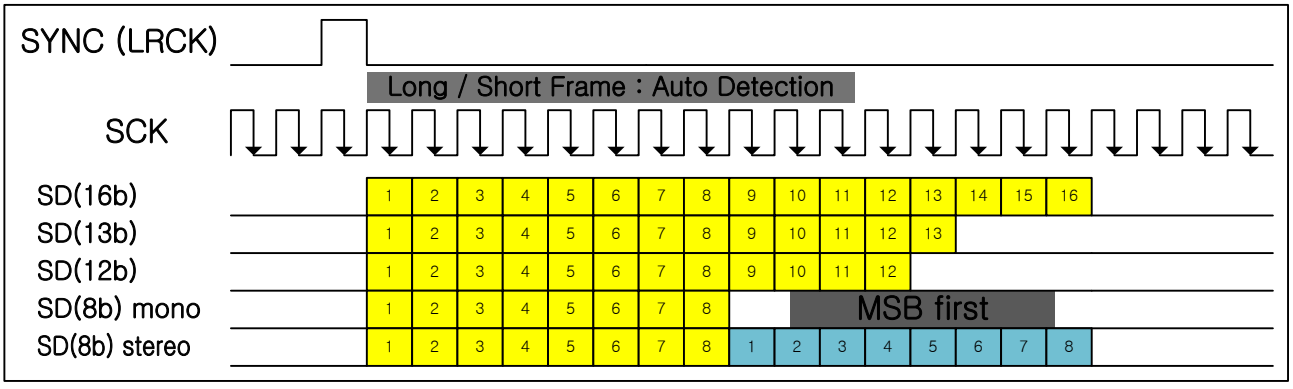
▶Long-frame Left-justified Interface format



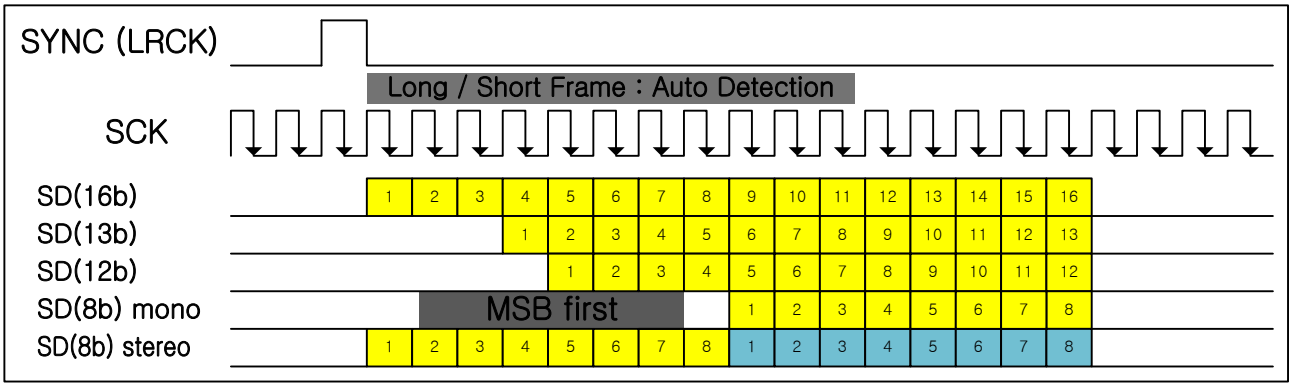
▶Long-frame Right-justified Interface format



▶Short-frame Left-justified Interface format

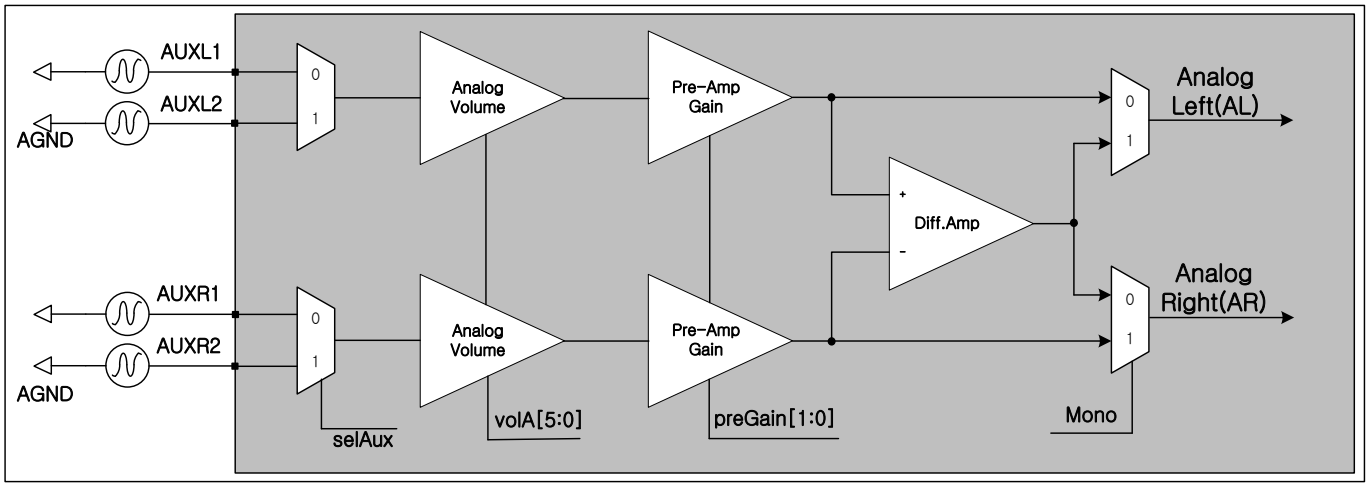


▶Short-frame Right-justified Interface format



4.3.4 Analog Audio Interface

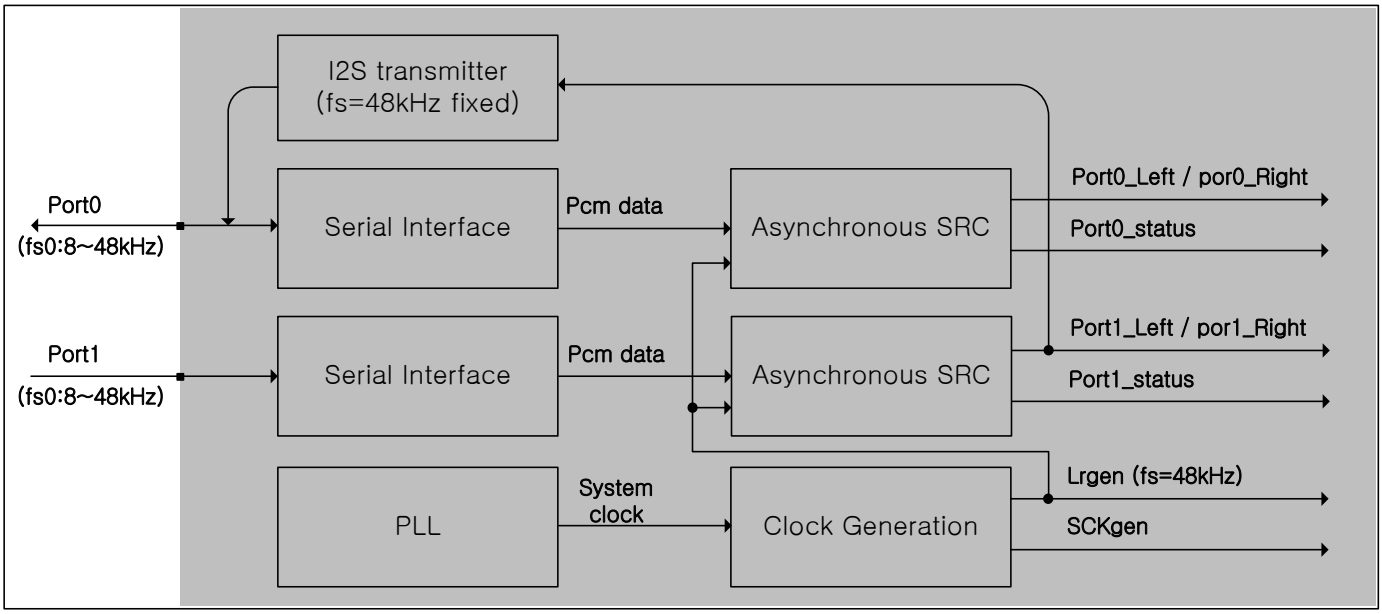
Independent 2-port stereo analog audio signals are selected by configuration of "selAux"(0x34.[0]) signal. Single-ended left / right input pins can be configured as differential input by "Mono" (0x34.[3]). At the differential input mode, left channel signal pin is positive input pin and right channel signal pin is negative input pin. Adjustable gain of pre-amplifier is 0/+6/+12/+18dB and range of analog volume is +16dB ~ -72dB. Total boosting gain of analog signal + 34dB therefore very small amplitude of analog signal can be handled without any external circuit. Analog volume table is shown in Appendix B.



4.4 Asynchronous Sample Rate Converter (ASRC)

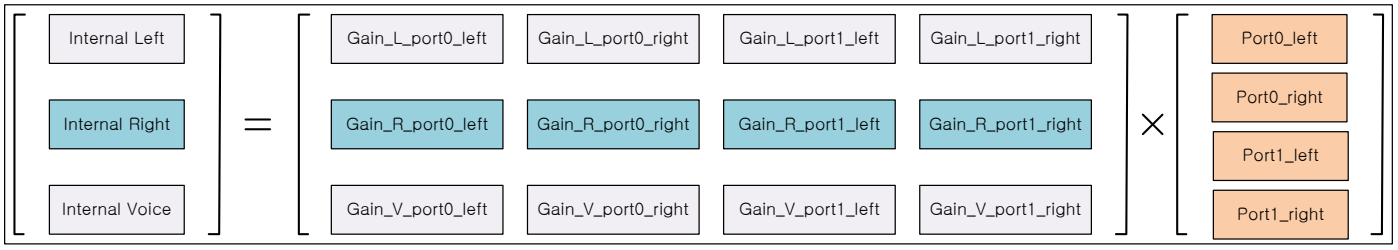
Range of input sampling frequency of port0 and port1 is 8~48kHz. Internal sampling frequency, fs(LRgen) is generated from system clock that is output frequency of internal PLL. Input digital audio data of port0 and port1 is re-sampled by asynchronous sample rate converter (ASRC) with fs=48kHz. Locking status (Lock0/Lock1) and input sampling frequency status (fs_port0[14:0]/fs_port1[14:0]) are provided and these values can be read out through only serial control interface I2C. Re-sampled audio data of port1 can be transmitted out through port0 (master mode of port0)

Sample frequency of port = fs_port[14:0]*48/2*2^{-12}[kHz]
If fs0=48kHz, then fs_port[14:0] = 0x2000
If fs0=44.1kHz, then fs_port[14:0] = 0x1D66
If fs0=32kHz, then fs_port[14:0] = 0x1555
If fs0=16kHz, then fs_port[14:0] = 0x0AAB
If fs0=8kHz, then fs_port[14:0] = 0x0555

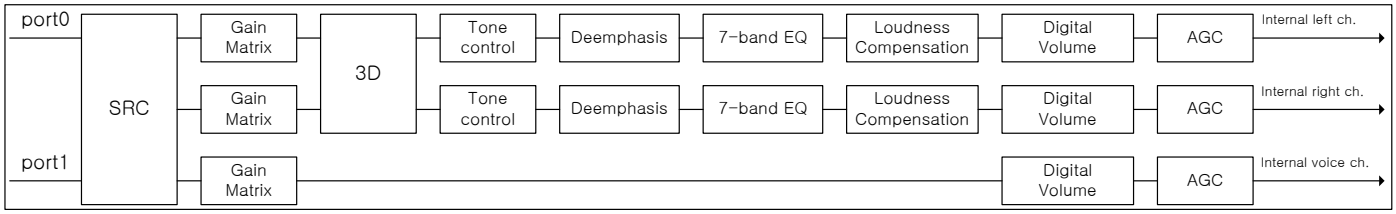


4.5 Input Gain Matrix

For digital audio signal processing, there are 3-processing channels internally; left / light / voice-channel. The sample-rate-converted audio data, port0_left / port0_right / port1_left / port1_right can be mixed down to generate internal 3-processing channel source by configuration of "input gain matrix". Mixing parameter consists of sign and gain. If sign is 0 (positive), mixing is additive in phase. If sign is 1(negative), mixing is additive 180° out-of-phase. Mixing level is configured by gain, and the range of gain is +24~-23.5dB, -∞ / 0.5dB step. Detailed Mixer gain is shown in Appendix C.



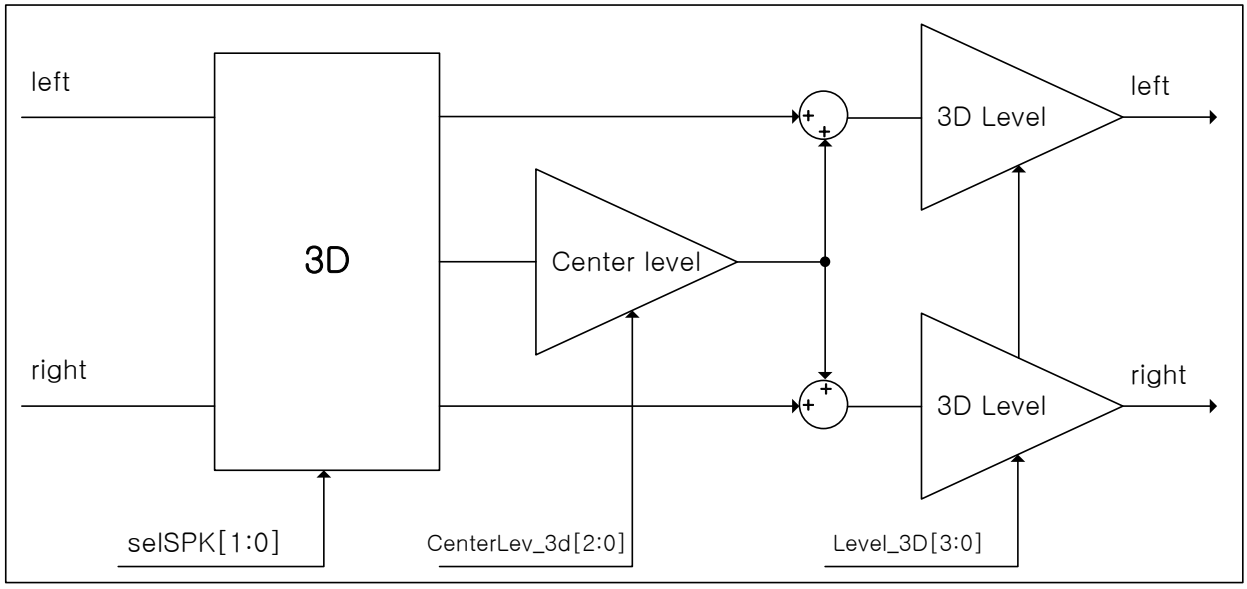
For internal left /right channel, there are various signal processing functions including 3D, but for voice channel, no extra signal processing except for volume and AGC function shown as follows:



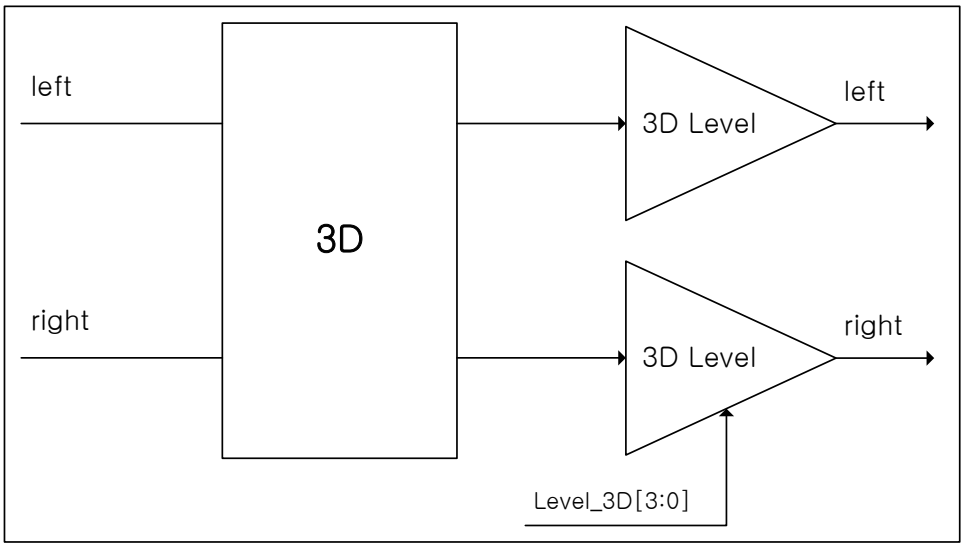
4.6 Stereo Enhanced 3D-Effect

Stereo enhanced 3D-effect function is implemented on this chip and there are 2 modes of 3D internally; one is loud speaker mode and the other is headphone mode. On/Off of 3D is controlled by "on3D" (0x2B.[0]) and internal mode is selected by "3Dmode" (0x2B.[1]).

Block diagram of 3D mode is shown below. "selSPK[1:0]" is selection of stereo speaker angle. "CenterLev_3D[2:0]" controls the sound level of virtual center position. "Level_3D[3:0]" controls the level of 3D-effect.



<Block diagram of loud speaker 3D mode>



<Block diagram of headphone 3D mode>

selSPK[1:0]	angle of stereo speakers
0	angle ≤ 5°
1	5° < angle ≤ 20°
2	20° < angle
3	Not used

<Selection of speaker angle at loud speaker 3D mode>

Level_3D[3:0]	Level of 3D-Effect		Level_3D[3:0]	Level of 3D-Effect	
	loud speaker mode	headphone mode		loud speaker mode	headphone mode
0	0.0	0.0	8	0.8	0.8
1	0.1	0.1	9	0.9	0.9
2	0.2	0.2	10	1.0	1.0
3	0.3	0.3	11	1.0	1.1
4	0.4	0.4	12	1.0	1.2
5	0.5	0.5	13	1.0	1.3
6	0.6	0.6	14	1.0	1.4
7	0.7	0.7	15	1.0	1.4

<Control of 3D Effect Level>

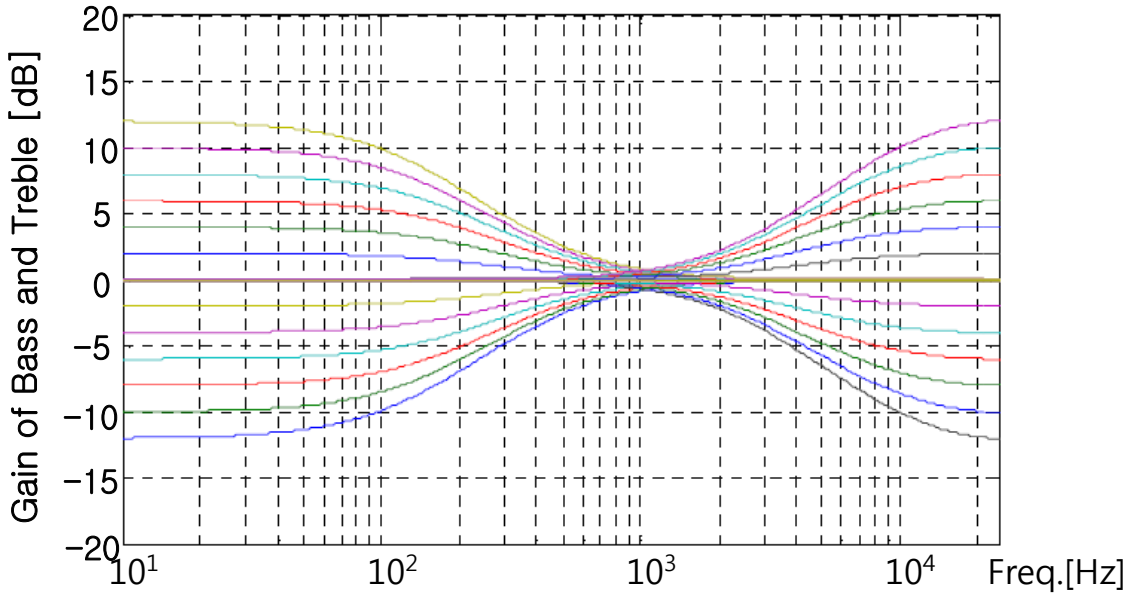
4.7 Tone Control (Bass and Treble)

Tone Control (Bass and Treble) is implemented on this chip. On/Off of Bass and Treble are controlled by "onBAS" (0x11.[0])and "onTRB" (0x11.[1]) independently. Transfer function of Bass is the same function of Treble :

$$H(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}}$$

Corner frequencies of Bass and Treble are 150Hz and 7Hz respectively. Range of adjustable gain is -12dB ~ +12dB / 2dB step. Detailed gain table is shown in Appendix D.

<Frequency Response of Bass and Treble>

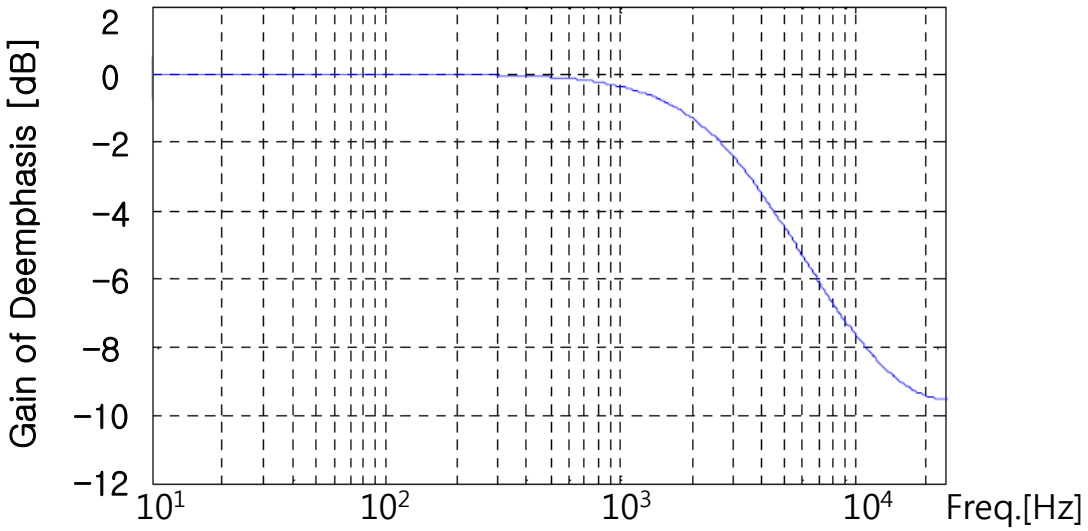


If the internal corner frequency or internal gain is not proper, an appropriate new coefficient set can be downloaded into this chip. To operate new coefficients normally, "onBAScustom" / "onTRBcustom" must be "On" after the completion of coefficients down-loading.

4.8 Deemphasis

Deemphasis filter is implemented on this chip and On/Off of Deemphasis filter is controlled by "onDE" (0x11.[2]). Time constants of pole and zero are 50us / 15us. Transfer function of deemphasis filter :

$$H(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}}$$



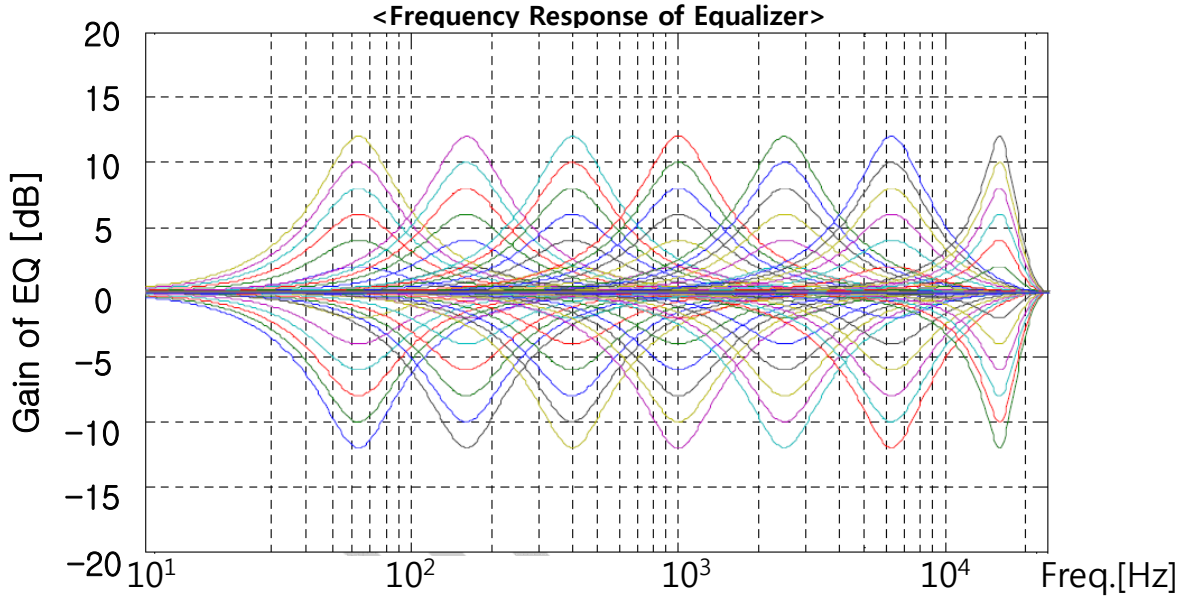
4.9 Equalizer (7-band)

7-band equalize is implemented on this chip. On/Off of each band of EQ is controlled by "onEQ[6:0]" (0x10.[6:0]) independently. Transfer function of each EQ :

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

Band	0	1	2	3	4	5	6
Center Frequency [Hz]	63	160	400	1000	2500	6300	16000

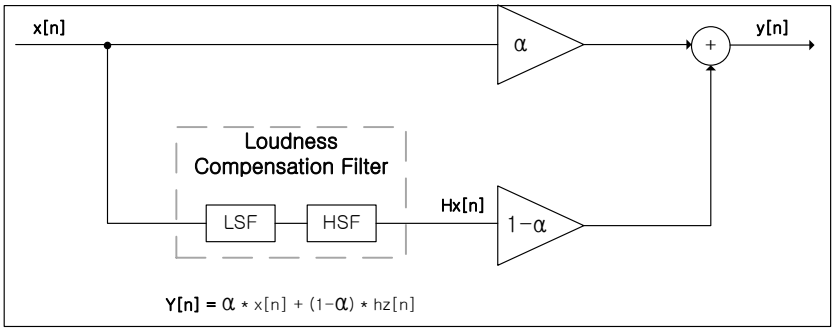
Range of adjustable gain is -12dB ~ +12dB / 2dB step. Detailed gain table is shown in Appendix D.



If the internal center frequency of internal gain is not proper, an appropriate coefficient set can be downloaded into this chip. To operate new coefficients normally. "onEQcustom[6:0]" must be "On" after the completion of coefficients down-loading.

4.10 Loudness Compensation

Loudness compensation is implemented on this chip. On/Off of Loudness compensation is controlled by "onLC" (0x11.[3]). Block diagram of loudness compensation is shown below :

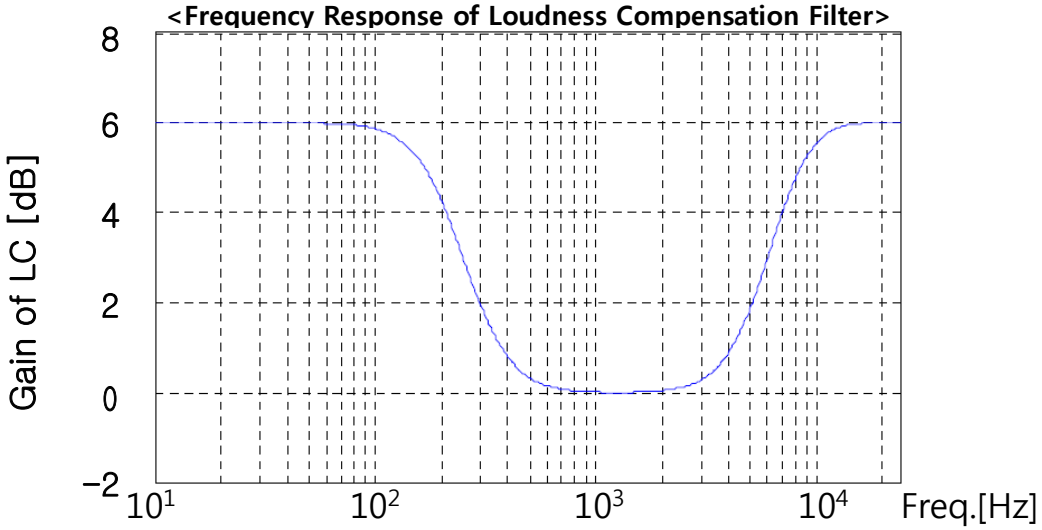


Transfer function of LSF and HSF :

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

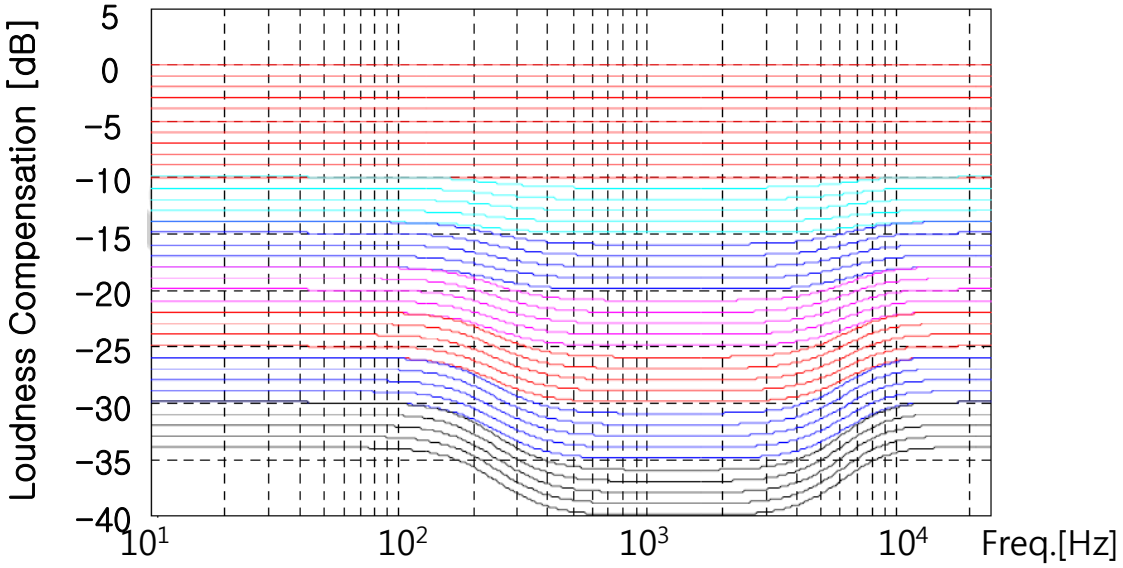
Output y[n] is the weighted sum of x[n] and hx[n] and the weighting factor α is determined by volume status.
Frequency responses of loudness compensation filter, LSH and HSF is shown below : corner frequency are 250Hz / 6kHz.

<Frequency Response of Loudness Compensation Filter>



Frequency responses of loudness compensation VS volume are shown below :

<Frequency Response of Loudness Compensation VS volume>

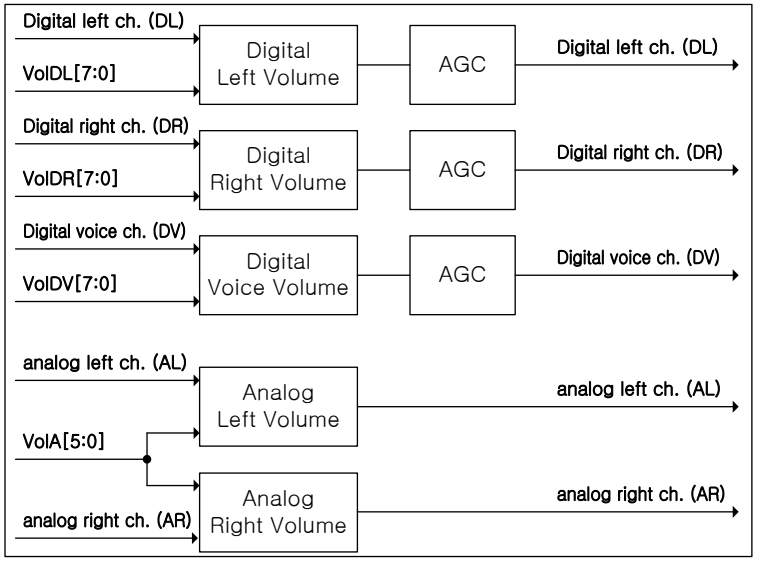


4.11 Volume and Mute Control

Digital volumes are supported for each digital audio source channel, DL (Digital Left) / DR (Digital Right) / DV (Digital Voice), independently. Volume registers are "volDL" (0x2D.[7:0]), "volDR" (0x2E.[7:0]), "volDV" (0x2F.[7:0]. Volume range is +24 ~ -75dB, -∞ and soft volume and soft mute are implemented by resolution of 0.25dB (by using interpolation method of 0.5dB volume table). Digital volume table is shown in Appendix A.

Analog volume is supported for analog audio source channel, AL (Analog Left) / AR (Analog Right) and left / right volume is independent with each other. Volume register is "volA" (0x35.[5:0] and volume range is +16 ~ -72dB, -∞ with 2dB step. Soft volume and soft mute are implemented by resolution of 2dB step. Analog volume table is shown in Appendix B.

Mute (0x01.[4]) is corresponding to -∞ volume operation and "Mute clear" is to operate in configured setting volume. Slopes of soft volume and soft mute are controlled by "muteTime[1:0]" (0x01.[3:2]) and "mclrTime[1:0]" (0x01.[1:0]).



muteTime[1:0] / mclrTime[1:0]	0	1	2	3
soft slop @ digital volume	21us/0.25dB	0.67ms/0.25dB	1.33ms/0.25dB	2.67ms/0.25dB
soft slop @ analog volume	31us/2dB	4ms/2dB	8ms/2dB	16ms/2dB

4.12 Automatic Gain Control (AGC)

Automatic gain control (AGC) is valid for only digital audio source channels, DL(Digital Left) / DR(Digital Right) / DV(Digital Voice). On/Off of AGC is controlled by "onAGC" (0x28.[7])" and configuration of expand mode is set by "onExpand" (0x28.[6]).

Attack time of AGC is set by "AttackTime[7:0]" (0x28.[5:0]) and is shown in Appendix F. Resolution of attack time is 21us/0.25dB and therefore corresponding time constant(τ) is 0.7ms / 8.68dB. Range of time constant is 0.7ms ~ 45.6ms.

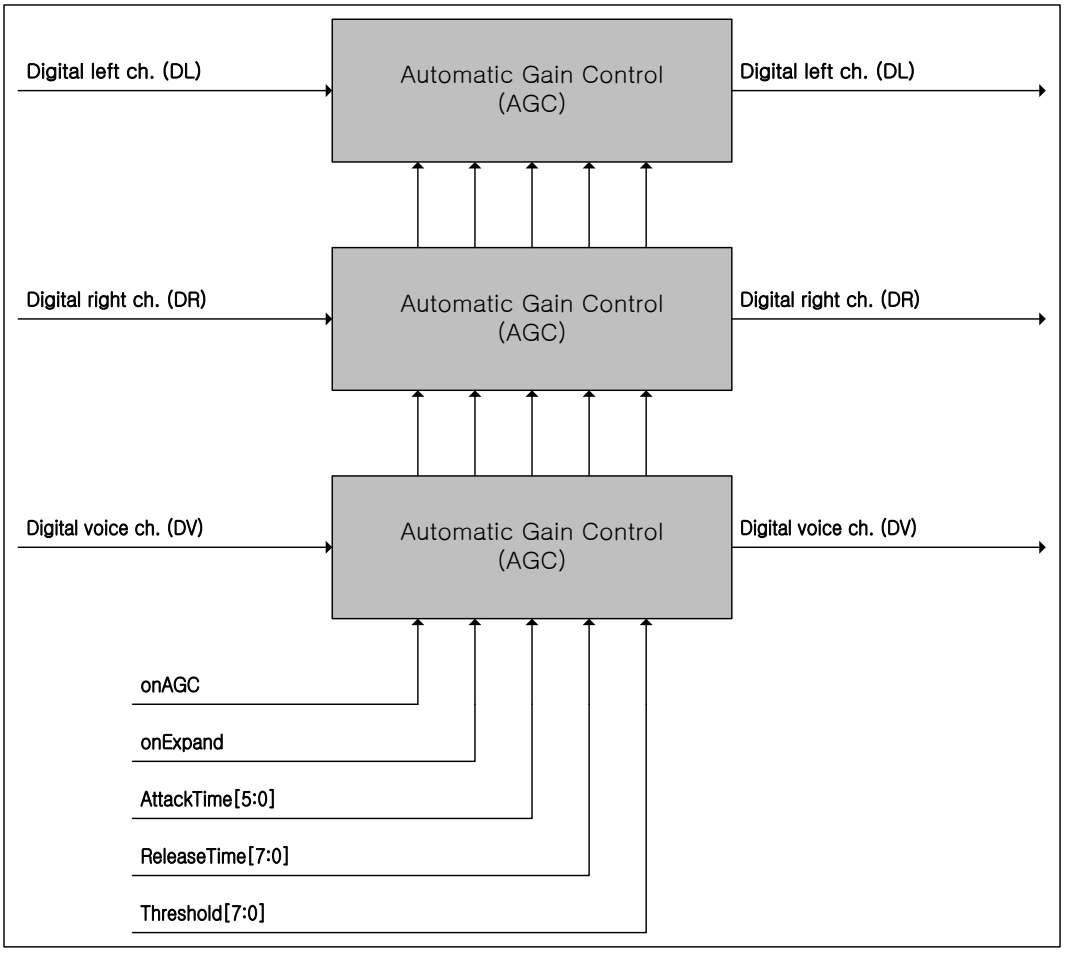
Release time of AGC is set by "ReleaseTime[7:0]" (0x29.[7:0]) and is shown in Appendix G. Resolution of release time is 333us /0.25dB and therefore corresponding time constant(τ) is 11.6ms / 8.68dB. Range of time constant is 0.01 ~ 2.95s.

Threshold level of AGC is set by "Threshold[7:0]" (0x2A.[7:0]) and is shown in Appendix H. Resolution of threshold level is 0.25dB. Range of threshold level is +24 ~ -39.75dB.

At AGC mode, there are two modes; one is "AGC expand mode" and the other is "AGC not-expand mode".

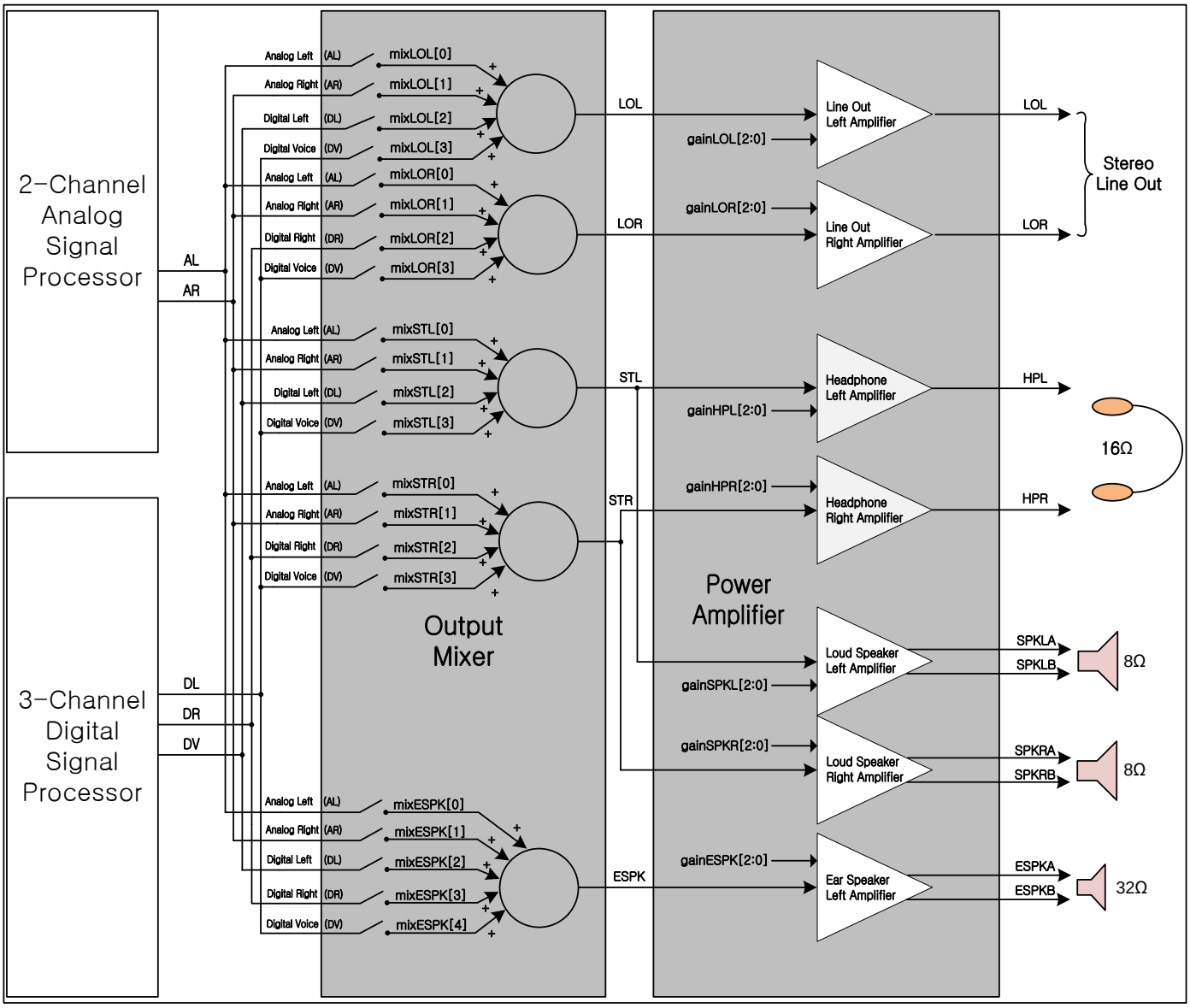
At AGC not-expand mode, internal volume is auto-controlled to limit the peak value of audio signal under the threshold level of AGC; that is, if peak value of audio is high, internal volume is adjusted down, but if peak value of audio signal is low, there is no auto-boosting volume.

At AGC expand mode, internal volume is auto-controlled to match the peak level of audio signal to threshold level of AGC; that is, if peak level of audio is high, internal volume is adjusted down, and if peak value of audio is low, then boosted up to the threshold level. In order to turn-on "AGC expand mode", turn on both "onAGC" and "onExpand".


Digital left ch. (DL)
Automatic Gain Control
(AGC)
Digital left ch. (DL)
Digital right ch. (DR)
Automatic Gain Control
(AGC)
Digital right ch. (DR)
Digital voice ch. (DV)
Automatic Gain Control
(AGC)
Digital voice ch. (DV)
onAGC
onExpand
AttackTime[5:0]
ReleaseTime[7:0]
Threshold[7:0]

4.13 Output Mixer and Power Amplifier

Internally there are 5-channel audio sources; Analog Left(AL), Analog Right(AR), Digital Left(DL), Digital Right(DR), Digital Voice(DV). Internal AL and AR audio source are originated from 2-port analog audio sources, AUXLx /AUXRx. Internal DL, DR, DV audio sources are originated from 2-port digital sources, LRCKx/SCKx/SDx. These internal 5-channel audio sources can be mixed to obtain LOL, LOR, STL, STR and ESPK signals. These mixed signals are amplified at output power amplifiers; line out left/right amplifier, headphone left/right amplifier, loud speaker left/right amplifier and ear speaker amplifier. Each power amplifier has an adjustable gain and the adjustable gain table is shown in Appendix E. Block diagram of output mixer and power amplifier is shown below:



In headphone application, DC-blocking capacitor is not necessary due to ground-referenced output. For ground-referenced output, it has negative power generated by charge-pump. Positive power for headphone amplifier is generated by LDO. Setting this LDO output value, headphone output power is capable to control. Also demodulation filter network is not needed in headphone application.

In loud speaker / ear speaker application, there is no need to connect demodulation filter network; filter-less application is available.

4.14 Coefficients Downloading of Various Filters

In case the internal coefficients of EQx, Bass and Treble filters are not proper, new appropriate coefficients can be downloaded into this chip through I2c/SPI interface. After completion of download, EQx custom mode can be turn-on to operate the filter with new coefficients.

Transfer function of each EQ :

$$H(z) = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}}$$

Transfer function of Bass and Treble are same :

$$H(z) = \frac{b_0 + b_1 z^{-1}}{1 + a_1 z^{-1}}$$

The coefficients of EQ filter are b0, b1, b2, -a1, -a2 and the coefficients of Bass or Treble filter are b0, b1, -a1. Data format of all coefficients is 3.21-format. 3 digit means bit number of integer part and 21 means bit number of fractional part. Therefore a coefficient is 3-byte length, that is, "coef0" consists of coef0_highByte, coef0_middleByte and coef0_lowByte. The system registers of coefficients are shown below :

Coef. Register Name	Coefficient		Address of system register		
	at EQx	at Bass / Treble	highByte	middleByte	lowByte
coef0	b0	b0	0x18	0x19	0x1A
coef1	b1	b1	0x1B	0x1C	0x1D
coef2	b2	-a1	0x1E	0x1F	0x20
coef3	-a1	-	0x21	0x22	0x23
coef4	-a2	-	0x24	0x25	0x26

Filter of custom mode si selected by "selFilter[3:0]" (0x27.[3:0] as shown below

Custom Filter	selFilter[3:0]
EQ0	0
EQ1	1
EQ2	2
EQ3	3
EQ4	4
EQ5	5
EQ6	6
Bass	7
Treble	8

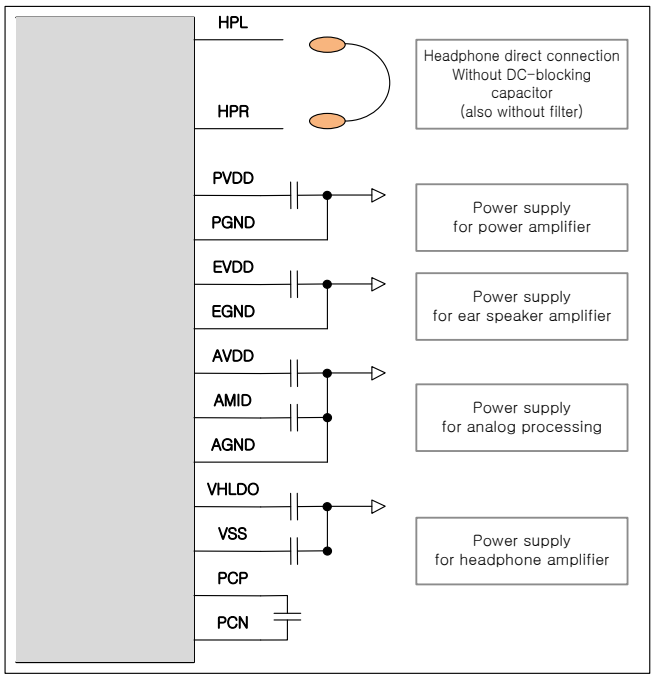
The downloaded filter coefficients to system register is moved by rising edge of "coefUpdate" (0x27.[4]) signal into the corresponding coefficient memory of the selected filter. Therefore after the completion of coefficient downloading, "selFilter[3:0]" and "coefUpdate" is configured properly. For next update cycle of coefficients, "coefUpdate" signal must be low after update cycle.

For example, if EQ3 is to be custom mode, transmit sequence is as follows :

① I2C start → transmit 0xDC(I2C device address) → transmit 0x18(system register address of coeff.) →
② transmit coef0_highByte → transmit coef0_middleByte → transmit coef0_lowByte →
③ transmit coef1_highByte → transmit coef1_middleByte → transmit coef1_lowByte →
④ transmit coef2_highByte → transmit coef2_middleByte → transmit coef2_lowByte →
⑤ transmit coef3_highByte → transmit coef3_middleByte → transmit coef3_lowByte →
⑥ transmit coef4_highByte → transmit coef4_middleByte → transmit coef4_lowByte →
⑦ transmit 0x13 (update and selection of EQ3) → transmit 0x03(for next update cycle) →
⑧ I2C end

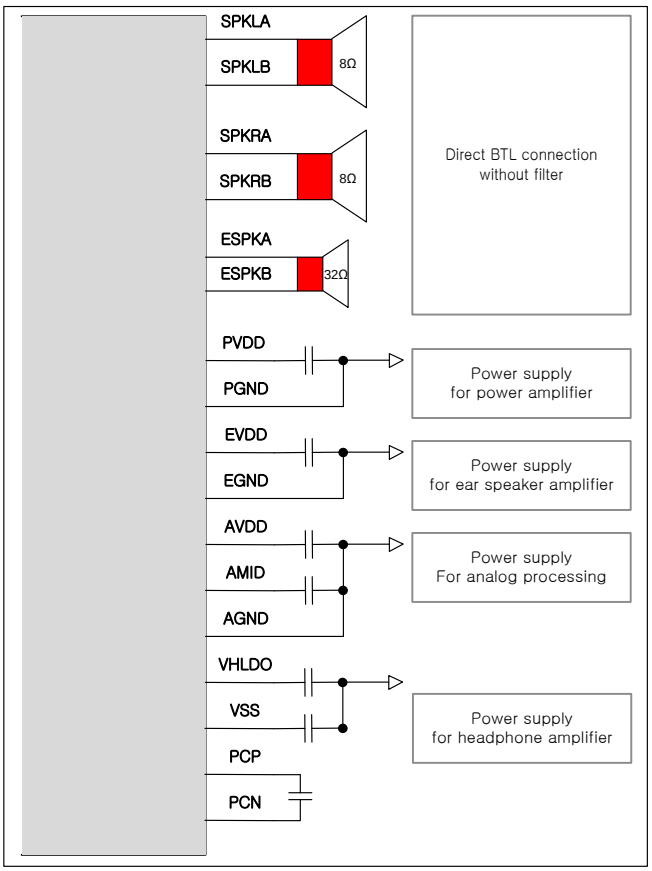
4.15.1 Amplifier Application

There are 4-types of output amplifiers; stereo line out amplifier, stereo headphone amplifier, stereo loud speaker amplifier and mono ear speaker amplifier. Line out amplifier has the capability to drive up to 600Ω load. On and Off control of amplifier operation is done by system register 0x49 as shown below. It is recommended that on/off configuration of "not-used amplifier" should be "off" for low power consumption.

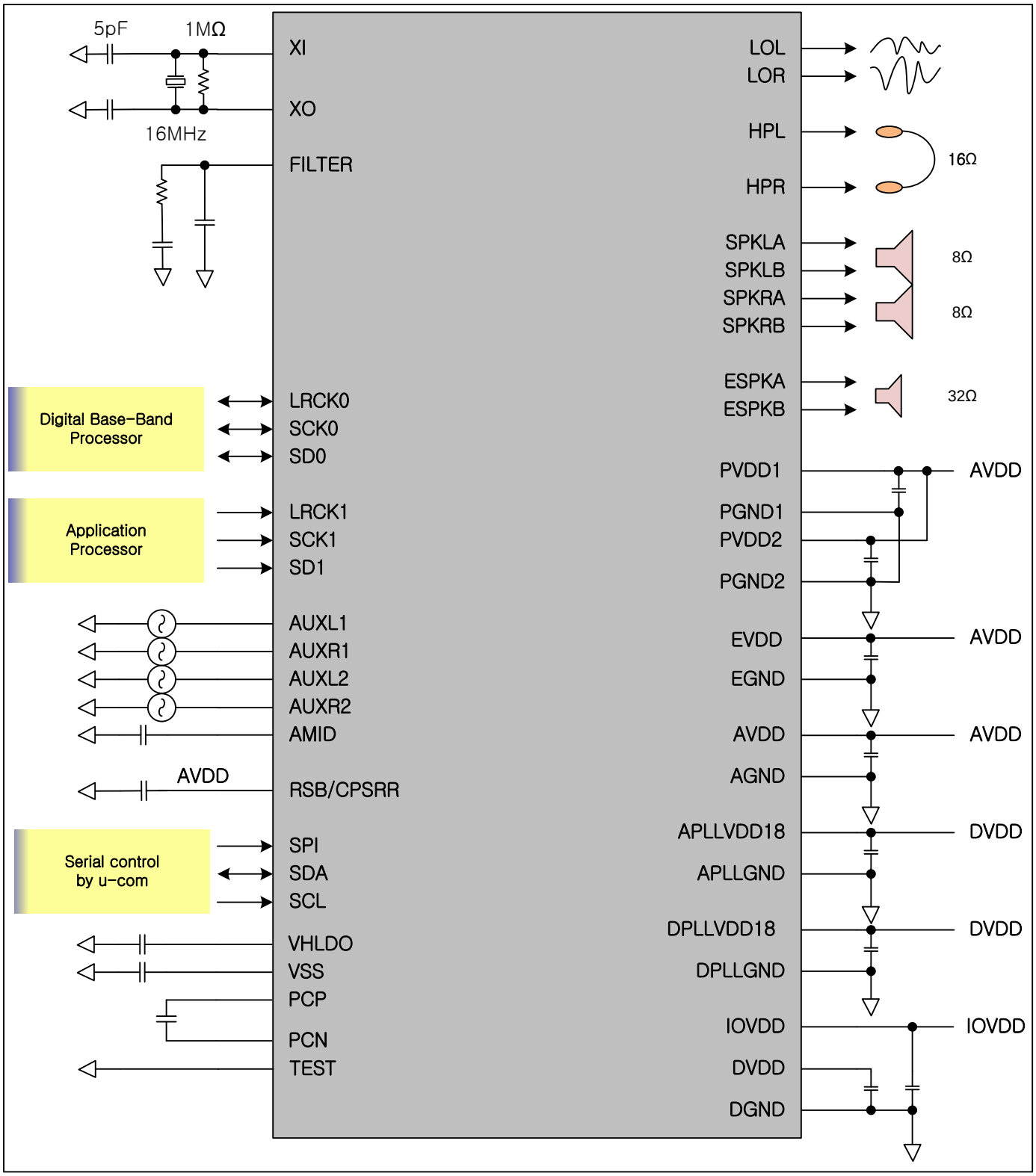


<Application without DC-blocking capacitor>

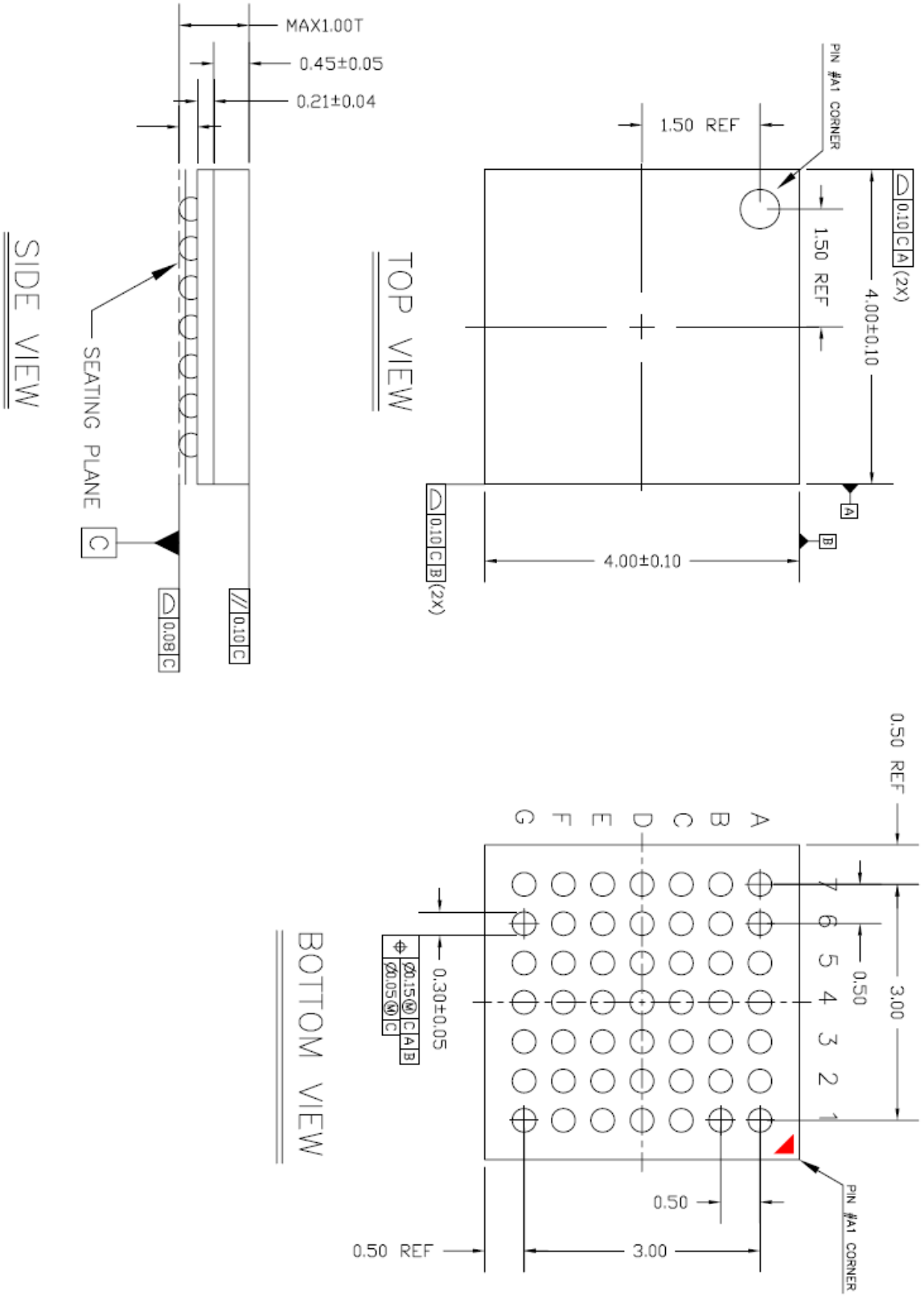
4.15.2 Stereo Loud Speaker and Mono Ear Speaker Application



5. APPLICATION CIRCUIT



6. PACKAGE DIMENSION



APPENDIX

Appendix A. Digital Volume Table

Register Value		Volume [dB]	Register Value		Volume [dB]	Register Value		Volume [dB]
Hex	Dec		Hex	Dec		Hex	Dec	
0x00	0	+24.0	0x40	64	-8.0	0x80	128	-40.0
0x01	1	+23.5	0x41	65	-8.5	0x81	129	-40.5
0x02	2	+23.0	0x42	66	-9.0	0x82	130	-41.0
0x03	3	+22.5	0x43	67	-9.5	0x83	131	-41.5
0x04	4	+22.0	0x44	68	-10.0	0x84	132	-42.0
0x05	5	+21.5	0x45	69	-10.5	0x85	133	-42.5
0x06	6	+21.0	0x46	70	-11.0	0x86	134	-43.0
0x07	7	+20.5	0x47	71	-11.5	0x87	135	-43.5
0x08	8	+20.	0x48	72	-12.0	0x88	136	-44.0
0x09	9	+19.5	0x49	73	-12.5	0x89	137	-44.5
0x0A	10	+19.0	0x4A	74	-13.0	0x8A	138	-45.0
0x0B	11	+18.5	0x4B	75	-13.5	0x8B	139	-45.5
0x0C	12	+18.0	0x4C	76	-14.0	0x8C	140	-46.0
0x0D	13	+17.5	0x4D	77	-14.5	0x8D	141	-47.0
0x0E	14	+17.0	0x4E	78	-15.0	0x8E	142	-48.0
0x0F	15	+16.5	0x4F	79	-15.5	0x8F	143	-49.0
0x10	16	+16.0	0x50	80	-16.0	0x90	144	-50.0
0x11	17	+15.5	0x51	81	-16.5	0x91	145	-51.0
0x12	18	+15.0	0x52	82	-17.0	0x92	146	-52.0
0x13	19	+14.5	0x53	83	-17.5	0x93	147	-53.0
0x14	20	+14.0	0x54	84	-18.0	0x94	148	-54.0
0x15	21	+13.5	0x55	85	-18.5	0x95	149	-55.0
0x16	22	+13.0	0x56	86	-19.0	0x96	150	-56.0
0x17	23	+12.5	0x57	87	-19.5	0x97	151	-57.0
0x18	24	+12.0	0x58	88	-20.0	0x98	152	-58.0
0x19	25	+11.5	0x59	89	-20.5	0x99	153	-60.0
0x1A	26	+11.0	0x5A	90	-21.0	0x9A	154	-62.0
0x1B	27	+10.5	0x5B	91	-21.5	0x9B	155	-64.0
0x1C	28	+10.0	0x5C	92	-22.0	0x9C	156	-66.0
0x1D	29	+9.5	0x5D	93	-22.5	0x9D	157	-69.0
0x1E	30	+9.0	0x5E	94	-23.0	0x9E	158	-72.0
0x1F	31	+8.5	0x5F	95	-23.5	0x9F	159	-75.0
0x20	32	+8.0	0x60	96	-24.0	0xA0~0xFF	160 ~ 255	-∞
0x21	33	+7.5	0x61	97	-24.5			
0x22	34	+7.0	0x62	98	-25.0			
0x23	35	+6.5	0x63	99	-25.5			
0x24	36	+6.0	0x64	100	-26.0			
0x25	37	+5.5	0x65	101	-26.5			
0x26	38	+5.0	0x66	102	-27.0			
0x27	39	+4.5	0x67	103	-27.5			
0x28	40	+4.0	0x68	104	-28.0			
0x29	41	+3.5	0x69	105	-28.5			
0x2A	42	+3.0	0x6A	106	-29.0			
0x2B	43	+2.5	0x6B	107	-29.5			
0x2C	44	+2.0	0x6C	108	-30.0			
0x2D	45	+1.5	0x6D	109	-30.5			
0x2E	46	+1.0	0x6E	110	-31.0			
0x2F	47	+0.5	0x6F	111	-31.5			
0x30	48	0.0	0x70	112	-32.0			
0x31	49	-0.5	0x71	113	-32.5			
0x32	50	-1.0	0x72	114	-33.0			
0x33	51	-1.5	0x73	115	-33.5			
0x34	52	-2.0	0x74	116	-34.0			
0x35	53	-2.5	0x75	117	-34.5			
0x36	54	-3.0	0x76	118	-35.0			
0x37	55	-3.5	0x77	119	-35.5			
0x38	56	-4.0	0x78	120	-36.0			
0x39	57	-4.5	0x79	121	-36.5			
0x3A	58	-5.0	0x7A	122	-37.0			
0x3B	59	-5.5	0x7B	123	-37.5			
0x3C	60	-6.0	0x7C	124	-38.0			
0x3D	61	-6.5	0x7D	125	-38.5			
0x3E	62	-7.0	0x7E	126	-39.0			
0x3F	63	-7.5	0x7F	127	-39.5			

Appendix B. Analog Volume Table

Register Value		Volume [dB]
Hex	Dec	
0x00	0	+16.0
0x01	1	+14.0
0x02	2	+12.0
0x03	3	+10.0
0x04	4	+8.0
0x05	5	+6.0
0x06	6	+4.0
0x07	7	+2.0
0x08	8	0.0
0x09	9	-2.0
0x0A	10	-4.0
0x0B	11	-6.0
0x0C	12	-8.0
0x0D	13	-10.0
0x0E	14	-12.0
0x0F	15	-14.0
0x00	16	-16.0
0x11	17	-18.0
0x12	18	-20.0
0x13	19	-22.0
0x14	20	-24.0
0x15	21	-26.0
0x16	22	-28.0
0x17	23	-30.0
0x18	24	-32.0
0x19	25	-34.0
0x1A	26	-36.0
0x1B	27	-38.0
0x1C	28	-40.0
0x1D	29	-42.0
0x1E	30	-44.0
0x1F	31	-46.0
0x20	32	-48.0
0x21	33	-50.0
0x22	34	-52.0
0x23	35	-54.0
0x24	36	-56.0
0x25	37	-58.0
0x26	38	-60.0
0x27	39	-62.0
0x28	40	-64.0
0x29	41	-66.0
0x2A	42	-68.0
0x2B	43	-70.0
0x2C	44	-72.0
0x2D	45	-∞

Appendix C. Mixer Gain Table

Register Value		Mixer Gain [dB]
Hex	Dec	
0x00	0	+24.0
0x01	1	+23.5
0x02	2	+23.0
0x03	3	+22.5
0x04	4	+22.0
0x05	5	+21.5
0x06	6	+21.0
0x07	7	+20.5
0x08	8	+20.0
0x09	9	+19.5
0x0A	10	+19.0
0x0B	11	+18.5
0x0C	12	+18.0
0x0D	13	+17.5
0x0E	14	+17.0
0x0F	15	+16.5
0x10	16	+16.0
0x11	17	+15.5
0x12	18	+15.0
0x13	19	+14.5
0x14	20	+14.0
0x15	21	+13.5
0x16	22	+13.0
0x17	23	+12.5
0x18	24	+12.0
0x19	25	+11.5
0x1A	26	+11.0
0x1B	27	+10.5
0x1C	28	+10.0
0x1D	29	+9.5
0x1E	30	+9.0
0x1F	31	+8.5
0x20	32	+8.0
0x21	33	+7.5
0x22	34	+7.0
0x23	35	+6.5
0x24	36	+6.0
0x25	37	+5.5
0x26	38	+5.0
0x27	39	+4.5
0x28	40	+4.0
0x29	41	+3.5
0x2A	42	+3.0
0x2B	43	+2.5
0x2C	44	+2.0
0x2D	45	+1.5
0x2E	46	+1.0
0x2F	47	+0.5
0x30	48	0.0
0x31	49	-0.5
0x32	50	-1.0
0x33	51	-1.5
0x34	52	-2.0
0x35	53	-2.5
0x36	54	-3.0
0x37	55	-3.5
0x38	56	-4.0
0x39	57	-4.5
0x3A	58	-5.0
0x3B	59	-5.5
0x3C	60	-6.0
0x3D	61	-6.5
0x3E	62	-7.0
0x3F	63	-7.5
0x40	64	-8.0
0x41	65	-8.5
0x42	66	-9.0
0x43	67	-9.5
0x44	68	-10.0
0x45	69	-10.5
0x46	70	-11.0
0x47	71	-11.5
0x48	72	-12.0
0x49	73	-12.5
0x4A	74	-13.0
0x4B	75	-13.5
0x4C	76	-14.0
0x4D	77	-14.5
0x4E	78	-15.0
0x4F	79	-15.5
0x50	80	-16.0
0x51	81	-16.5
0x52	82	-17.0
0x53	83	-17.5
0x54	84	-18.0
0x55	85	-18.5
0x56	86	-19.0
0x57	87	-19.5
0x58	88	-20.0
0x59	89	-20.5
0x5A	90	-21.0
0x5B	91	-21.5
0x5C	92	-22.0
0x5D	93	-22.5
0x5E	94	-23.0
0x5F	95	-23.5
0x60	93	-∞

Appendix D. Filter Gain Table

Register Value		Filter Gain [dB]
Hex	Dec	
0x00	0	-12
0x01	1	-10
0x02	2	-8
0x03	3	-6
0x04	4	-4
0x05	5	-2
0x06	6	0
0x07	7	+2
0x08	8	+4
0x09	9	+6
0x0A	10	+8
0x0B	11	+10
0x0C	12	+12

Appendix E. Adjustable Gain Table of Power Amplifier

Register Value		Adjustable Gain [dB]	
Hex	Dec	of Headphone Amplifier	of the others
0x00	0	-6	0
0x01	1	-8	-2
0x02	2	-10	-4
0x03	3	-12	-6
0x04	4	-14	-8
0x05	5	-16	-10
0x06	6	-18	-12
0x07	7	-20	-14

Appendix F. Attack Time Table of AGC

Register Value		time/0.25dB [ms]	time constant (time/8.68dB) [ms]	Register Value		time/0.25dB [ms]	time constant (time/8.68dB) [ms]
Hex	Dec			Hex	Dec		
0x00	0	0.02	0.7	0x20	32	0.67	23.1
0x01	1	0.02	0.7	0x21	33	0.69	23.9
0x02	2	0.04	1.4	0x22	34	0.71	24.6
0x03	3	0.06	2.2	0x23	35	0.73	25.3
0x04	4	0.08	2.9	0x24	36	0.75	26.0
0x05	5	0.10	3.6	0x25	37	0.77	26.8
0x06	6	0.13	4.3	0x26	38	0.79	27.5
0x07	7	0.15	5.1	0x27	39	0.81	28.2
0x08	8	0.17	5.8	0x28	40	0.83	28.9
0x09	9	0.19	6.5	0x29	41	0.85	29.7
0x0A	10	0.21	7.2	0x2A	42	0.88	30.4
0x0B	11	0.23	8.0	0x2B	43	0.90	31.1
0x0C	12	0.25	8.7	0x2C	44	0.92	31.8
0x0D	13	0.27	9.4	0x2D	45	0.94	32.6
0x0E	14	0.29	10.1	0x2E	46	0.96	33.3
0x0F	15	0.31	10.9	0x2F	47	0.98	34.0
0x10	16	0.33	11.6	0x30	48	1.00	34.7
0x11	17	0.35	12.3	0x31	49	1.02	35.4
0x12	18	0.38	13.0	0x32	50	1.04	36.2
0x13	19	0.40	13.7	0x33	51	1.06	36.9
0x14	20	0.45	14.5	0x34	52	1.08	37.6
0x15	21	0.44	15.2	0x35	53	1.10	38.3
0x16	22	0.46	15.9	0x36	54	1.13	39.1
0x17	23	0.48	16.6	0x37	55	1.15	39.8
0x18	24	0.50	17.4	0x38	56	1.17	40.5
0x19	25	0.52	18.1	0x39	57	1.19	41.2
0x1A	26	0.54	18.8	0x3A	58	1.21	42.0
0x1B	27	0.56	19.5	0x3B	59	1.23	42.7
0x1C	28	0.58	20.3	0x3C	60	1.25	43.4
0x1D	29	0.60	21.0	0x3D	61	1.27	44.4
0x1E	30	0.63	21.7	0x3E	62	1.29	44.8
0x1F	31	0.65	22.4	0x3F	63	1.31	45.6

Appendix G. Release Time Table of AGC

Register Val.		time /0.25dB [ms]	time constant (time/8.68dB) [s]	Register Val.		time /0.25dB [ms]	time constant (time/8.68dB) [s]	Register Val.		time /0.25dB [ms]	time constant (time/8.68dB) [s]	Register Val.		time /0.25dB [ms]	time constant (time/8.68dB) [s]
Hex	Dec			Hex	Dec			Hex	Dec			Hex	Dec		
0x00	0	0.33	0.01	0x40	64	21.33	0.74	0x80	128	42.67	1.48	0xC0	192	64.00	2.22
0x01	1	0.33	0.01	0x41	65	21.67	0.75	0x81	129	43.00	1.49	0xC1	193	64.33	2.23
0x02	2	0.67	0.02	0x42	66	22.00	0.76	0x82	130	43.33	1.50	0xC2	194	64.67	2.25
0x03	3	1.00	0.03	0x43	67	22.33	0.78	0x83	131	43.67	1.52	0xC3	195	65.00	2.26
0x04	4	1.33	0.05	0x44	68	22.67	0.79	0x84	132	44.00	1.53	0xC4	196	65.33	2.27
0x05	5	1.67	0.06	0x45	69	23.00	0.80	0x85	133	44.33	1.54	0xC5	197	65.67	2.28
0x06	6	2.00	0.07	0x46	70	23.33	0.81	0x86	134	44.67	1.55	0xC6	198	66.00	2.29
0x07	7	2.33	0.08	0x47	71	23.67	0.82	0x87	135	45.00	1.56	0xC7	199	66.33	2.30
0x08	8	2.67	0.09	0x48	72	24.00	0.83	0x88	136	45.33	1.57	0xC8	200	66.67	2.31
0x09	9	3.00	0.10	0x49	73	24.33	0.84	0x89	137	45.67	1.59	0xC9	201	67.00	2.33
0x0A	10	3.33	0.12	0x4A	74	24.67	0.86	0x8A	138	46.00	1.60	0xCA	202	67.33	2.34
0x0B	11	3.67	0.13	0x4B	75	25.00	0.87	0x8B	139	46.33	1.61	0xCB	203	67.67	2.35
0x0C	12	4.00	0.14	0x4C	76	25.33	0.88	0x8C	140	46.67	1.62	0xCC	204	68.00	2.36
0x0D	13	4.33	0.15	0x4D	77	25.67	0.89	0x8D	141	47.00	1.63	0xCD	205	68.33	2.37
0x0E	14	4.67	0.16	0x4E	78	26.00	0.90	0x8E	142	47.33	1.64	0xCE	206	68.67	2.38
0x0F	15	5.00	0.17	0x4F	79	26.33	0.91	0x8F	143	47.67	1.65	0xCF	207	69.00	2.40
0x10	16	5.33	0.19	0x50	80	26.67	0.93	0x90	144	48.00	1.67	0xD0	208	69.33	2.41
0x11	17	5.67	0.20	0x51	81	27.00	0.94	0x91	145	48.33	1.68	0xD1	209	69.67	2.42
0x12	18	6.00	0.21	0x52	82	27.33	0.95	0x92	146	48.67	1.69	0xD2	210	70.00	2.43
0x13	19	6.33	0.22	0x53	83	27.67	0.96	0x93	147	49.00	1.70	0xD3	211	70.33	2.44
0x14	20	6.67	0.23	0x54	84	28.00	0.97	0x94	148	49.33	1.71	0xD4	212	70.67	2.45
0x15	21	7.00	0.24	0x55	85	28.33	0.98	0x95	149	49.67	1.72	0xD5	213	71.00	2.47
0x16	22	7.33	0.25	0x56	86	28.67	1.00	0x96	150	50.00	1.74	0xD6	214	71.33	2.48
0x17	23	7.67	0.27	0x57	87	29.00	1.01	0x97	151	50.33	1.75	0xD7	215	71.67	2.49
0x18	24	8.00	0.28	0x58	88	29.33	1.02	0x98	152	50.67	1.76	0xD8	216	72.00	2.50
0x19	25	8.33	0.29	0x59	89	29.67	1.03	0x99	153	51.00	1.77	0xD9	217	72.33	2.51
0x1A	26	8.67	0.30	0x5A	90	30.00	1.04	0x9A	154	51.33	1.78	0xDA	218	72.67	2.52
0x1B	27	9.00	0.31	0x5B	91	30.33	1.05	0x9B	155	51.67	1.79	0xDB	219	73.00	2.53
0x1C	28	9.33	0.32	0x5C	92	30.67	1.06	0x9C	156	52.00	1.81	0xDC	220	73.33	2.55
0x1D	29	9.67	0.34	0x5D	93	31.00	1.08	0x9D	157	52.33	1.82	0xDD	221	73.67	2.56
0x1E	30	10.00	0.35	0x5E	94	31.33	1.09	0x9E	158	52.67	1.83	0xDE	222	74.00	2.57
0x1F	31	10.33	0.36	0x5F	95	31.67	1.10	0x9F	159	53.00	1.84	0xDF	223	74.33	2.58
0x20	32	10.67	0.37	0x60	96	32.00	1.11	0xA0	160	53.33	1.85	0xE0	224	74.67	2.59
0x21	33	11.00	0.38	0x61	97	32.33	1.12	0xA1	161	53.67	1.86	0xE1	225	75.00	2.60
0x22	34	11.33	0.39	0x62	98	32.67	1.13	0xA2	162	54.00	1.87	0xE2	226	75.33	2.62
0x23	35	11.67	0.41	0x63	99	33.00	1.15	0xA3	163	54.33	1.89	0xE3	227	75.67	2.63
0x24	36	12.00	0.42	0x64	100	33.33	1.16	0xA4	164	54.67	1.90	0xE4	228	76.00	2.64
0x25	37	12.33	0.43	0x65	101	33.67	1.17	0xA5	165	55.00	1.91	0xE5	229	76.33	2.65
0x26	38	12.67	0.44	0x66	102	34.00	1.18	0xA6	166	55.33	1.92	0xE6	230	76.67	2.66
0x27	39	13.00	0.45	0x67	103	34.33	1.19	0xA7	167	55.67	1.93	0xE7	231	77.00	2.67
0x28	40	13.33	0.46	0x68	104	34.67	1.20	0xA8	168	56.00	1.94	0xE8	232	77.33	2.67
0x29	41	13.67	0.47	0x69	105	35.00	1.22	0xA9	169	56.33	1.96	0xE9	233	77.67	2.70
0x2A	42	14.00	0.49	0x6A	106	35.33	1.23	0xAA	170	56.67	1.97	0xEA	234	78.00	2.71
0x2B	43	14.33	0.50	0x6B	107	35.67	1.24	0xAB	171	57.00	1.98	0xEB	235	78.33	2.72
0x2C	44	14.67	0.51	0x6C	108	36.00	1.25	0xAC	172	57.33	1.99	0xEC	236	78.67	2.73
0x2D	45	15.00	0.52	0x6D	109	36.33	1.26	0xAD	173	57.67	2.00	0xED	237	79.00	2.74
0x2E	46	15.33	0.53	0x6E	110	36.67	1.27	0xAE	174	58.00	2.01	0xEE	238	79.33	2.75
0x2F	47	15.67	0.54	0x6F	111	37.00	1.28	0xAF	175	58.33	203	0xEF	239	79.67	2.77
0x30	48	16.00	0.56	0x70	112	37.33	1.30	0xB0	176	58.67	2.04	0xF0	240	80.00	2.78
0x31	49	16.33	0.57	0x71	113	37.67	1.31	0xB1	177	59.00	2.05	0xF1	241	80.33	2.79
0x32	50	16.67	0.58	0x72	114	38.00	1.32	0xB2	178	59.33	2.06	0xF2	242	80.67	2.80
0x33	51	17.00	0.59	0x73	115	38.33	1.33	0xB3	179	59.67	2.07	0xF3	243	81.00	2.81
0x34	52	17.33	0.60	0x74	116	38.67	1.34	0xB4	180	60.00	2.08	0xF4	244	81.33	2.82
0x35	53	17.67	0.61	0x75	117	39.00	1.35	0xB5	181	60.33	2.09	0xF5	245	81.67	2.84
0x36	54	18.00	0.62	0x76	118	39.33	1.37	0xB6	182	60.67	2.11	0xF6	246	82.00	2.85
0x37	55	18.33	0.64	0x77	119	39.67	1.38	0xB7	183	61.00	2.12	0xF7	247	82.33	2.86
0x38	56	18.67	0.65	0x78	120	40.00	1.39	0xB8	184	61.33	2.13	0xF8	248	82.67	2.87
0x39	57	19.00	0.66	0x79	121	40.33	1.40	0xB9	185	61.67	2.14	0xF9	249	83.00	2.88
0x3A	58	19.33	0.67	0x7A	122	40.67	1.41	0xBA	186	62.00	2.15	0xFA	250	83.33	2.89
0x3B	59	19.67	0.68	0x7B	123	41.00	1.42	0xBB	187	62.33	2.16	0xFB	251	83.67	2.90
0x3C	60	20.00	0.69	0x7C	124	41.33	1.44	0xBC	188	62.67	2.18	0xFC	252	84.00	2.92
0x3D	61	20.33	0.71	0x7D	125	41.67	1.45	0xBD	189	63.00	2.19	0xFD	253	84.33	2.93
0x3E	62	20.67	0.72	0x7E	126	42.00	1.46	0xBE	190	63.33	2.20	0xFE	254	84.67	2.94
0x3F	63	21.00	0.73	0x7F	127	42.33	1.47	0xBF	191	63.67	2.21	0xFF	255	85.00	2.895

Appendix h. Threshold Level Table of AGC

Register Val.		Threshold level [dB]	Register Val		Threshold level [dB]	Register Val		Threshold level [dB]	Register Val		Threshold level [dB]
Hex	Dec		Hex	Dec		Hex	Dec		Hex	Dec	
0x00	0	+24.00	0x40	64	+8.00	0x80	128	-8.00	0xC0	192	-24.00
0x01	1	+23.75	0x41	65	+7.75	0x81	129	-8.25	0xC1	193	-24.25
0x02	2	+23.50	0x42	66	+7.50	0x82	130	-8.50	0xC2	194	-24.50
0x03	3	+23.25	0x43	67	+7.25	0x83	131	-8.75	0xC3	195	-24.75
0x04	4	+23.00	0x44	68	+7.00	0x84	132	-9.00	0xC4	196	-25.00
0x05	5	+22.75	0x45	69	+6.75	0x85	133	-9.25	0xC5	197	-25.25
0x06	6	+22.50	0x46	70	+6.50	0x86	134	-9.50	0xC6	198	-25.50
0x07	7	+22.25	0x47	71	+6.25	0x87	135	-9.75	0xC7	199	-25.75
0x08	8	+22.00	0x48	72	+6.00	0x88	136	-10.00	0xC8	200	-26.00
0x09	9	+21.75	0x49	73	+5.75	0x89	137	-10.25	0xC9	201	-26.25
0x0A	10	+21.50	0x4A	74	+5.50	0x8A	138	-10.50	0xCA	202	-26.50
0x0B	11	+21.25	0x4B	75	+5.25	0x8B	139	-10.75	0xCB	203	-26.75
0x0C	12	+21.00	0x4C	76	+5.00	0x8C	140	-11.00	0xCC	204	-27.00
0x0D	13	+20.75	0x4D	77	+4.75	0x8D	141	-11.25	0xCD	205	-27.25
0x0E	14	+20.50	0x4E	78	+4.50	0x8E	142	-11.50	0xCE	206	-27.50
0x0F	15	+20.25	0x4F	79	+4.25	0x8F	143	-11.75	0xCF	207	-27.75
0x10	16	+20.00	0x50	80	+4.00	0x90	144	-12.00	0xD0	208	-28.00
0x11	17	+19.75	0x51	81	+3.75	0x91	145	-12.25	0xD1	209	-28.25
0x12	18	+19.50	0x52	82	+3.50	0x92	146	-12.50	0xD2	210	-28.50
0x13	19	+19.25	0x53	83	+3.25	0x93	147	-12.75	0xD3	211	-28.75
0x14	20	+19.00	0x54	84	+3.00	0x94	148	-13.00	0xD4	212	-29.00
0x15	21	+18.75	0x55	85	+2.75	0x95	149	-13.25	0xD5	213	-29.25
0x16	22	+18.50	0x56	86	+2.50	0x96	150	-13.50	0xD6	214	-29.50
0x17	23	+18.25	0x57	87	+2.25	0x97	151	-13.75	0xD7	215	-29.75
0x18	24	+18.00	0x58	88	+2.00	0x98	152	-14.00	0xD8	216	-30.00
0x19	25	+17.75	0x59	89	+1.75	0x99	153	-14.25	0xD9	217	-30.25
0x1A	26	+17.50	0x5A	90	+1.50	0x9A	154	-14.50	0xDA	218	-30.50
0x1B	27	+17.25	0x5B	91	+1.25	0x9B	155	-14.75	0xDB	219	-30.75
0x1C	28	+17.00	0x5C	92	+1.00	0x9C	156	-15.00	0xDC	220	-31.00
0x1D	29	+16.75	0x5D	93	+0.75	0x9D	157	-15.25	0xDD	221	-31.25
0x1E	30	+16.50	0x5E	94	+0.50	0x9E	158	-15.50	0xDE	222	-31.50
0x1F	31	+16.25	0x5F	95	+0.25	0x9F	159	-15.75	0xDF	223	-31.75
0x20	32	+16.00	0x60	96	0.00	0xA0	160	-16.00	0xE0	224	-32.00
0x21	33	+15.75	0x61	97	-0.25	0xA1	161	-16.25	0xE1	225	-32.25
0x22	34	+15.50	0x62	98	-0.50	0xA2	162	-16.50	0xE2	226	-32.50
0x23	35	+15.25	0x63	99	-0.70	0xA3	163	-16.75	0xE3	227	-32.75
0x24	36	+15.00	0x64	100	-1.00	0xA4	164	-17.00	0xE4	228	-33.00
0x25	37	+14.75	0x65	101	-1.25	0xA5	165	-17.25	0xE5	229	-33.25
0x26	38	+14.50	0x66	102	-1.50	0xA6	166	-17.50	0xE6	230	-33.50
0x27	39	+14.25	0x67	103	-1.75	0xA7	167	-17.75	0xE7	231	-33.75
0x28	40	+14.00	0x68	104	-2.00	0xA8	168	-18.00	0xE8	232	-34.00
0x29	41	+13.75	0x69	105	-2.25	0xA9	169	-18.25	0xE9	233	-34.25
0x2A	42	+13.50	0x6A	106	-2.50	0xAA	170	-18.50	0xEA	234	-34.50
0x2B	43	+13.25	0x6B	107	-2.75	0xAB	171	-18.75	0xEB	235	-34.75
0x2C	44	+13.00	0x6C	108	-3.00	0xAC	172	-19.00	0xEC	236	-35.00
0x2D	45	+12.75	0x6D	109	-3.25	0xAD	173	-19.25	0xED	237	-35.25
0x2E	46	+12.50	0x6E	110	-3.50	0xAE	174	-19.50	0xEE	238	-35.50
0x2F	47	+12.25	0x6F	111	-3.75	0xAF	175	-19.75	0xEF	239	-35.75
0x30	48	+12.00	0x70	112	-4.00	0xB0	176	-20.00	0xF0	240	-36.00
0x31	49	+11.75	0x71	113	-4.25	0xB1	177	-20.25	0xF1	241	-36.25
0x32	50	+11.50	0x72	114	-4.50	0xB2	178	-20.50	0xF2	242	-36.50
0x33	51	+11.25	0x73	115	-4.75	0xB3	179	-20.75	0xF3	243	-36.75
0x34	52	+11.00	0x74	116	-5.00	0xB4	180	-21.00	0xF4	244	-37.00
0x35	53	+10.75	0x75	117	-5.25	0xB5	181	-21.25	0xF5	245	-37.25
0x36	54	+10.50	0x76	118	-5.50	0xB6	182	-21.50	0xF6	246	-37.50
0x37	55	+10.25	0x77	119	-5.75	0xB7	183	-21.75	0xF7	247	-37.75
0x38	56	+10.00	0x78	120	-6.00	0xB8	184	-22.00	0xF8	248	-38.00
0x39	57	+9.75	0x79	121	-6.25	0xB9	185	-22.25	0xF9	249	-38.25
0x3A	58	+9.50	0x7A	122	-6.50	0xBA	186	-22.50	0xFA	250	-38.50
0x3B	59	+9.25	0x7B	123	-6.75	0xBB	187	-22.75	0xFB	251	-38.75
0x3C	60	+9.00	0x7C	124	-7.00	0xBC	188	-23.00	0xFC	252	-39.00
0x3D	61	+8.75	0x7D	125	-7.25	0xBD	189	-23.25	0xFD	253	-39.25
0x3E	62	+8.50	0x7E	126	-7.50	0xBE	190	-23.50	0xFE	254	-39.50
0x3F	63	+8.25	0x7F	127	-7.75	0xBF	191	-23.75	0xFF	255	-39.75